EE 330
Lecture 7

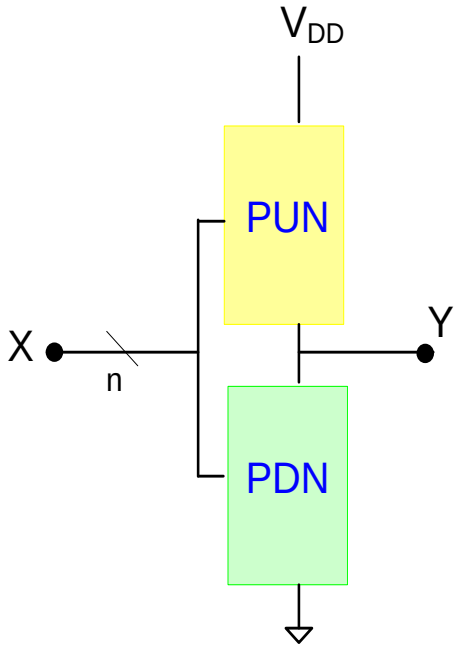
- Propagation Delay
- Stick Diagrams
- Technology Files
  - Design Rules

As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Review from Last Time

Complex Gates



Complex Gate Design Strategy:

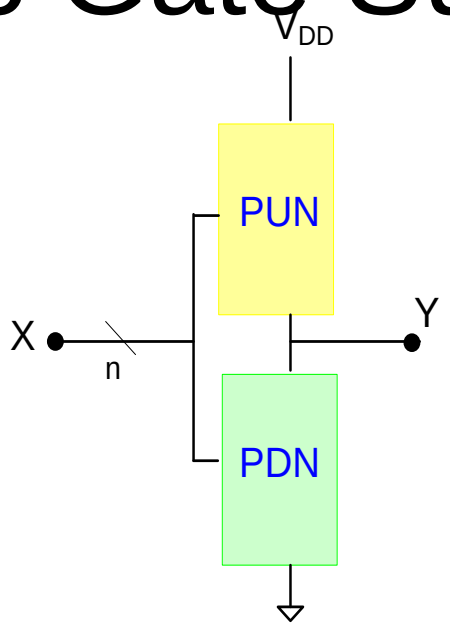
1. Implement $\overline{Y}$ in the PDN

2. Implement Y in the PUN (must complement the input variables since p-channel devices are used)

(Y and $\overline{Y}$ often expressed in either SOP or POS form)

Review from Last Time

Complex Logic Gate Summary:



If PUN and PDN satisfy the characteristics:

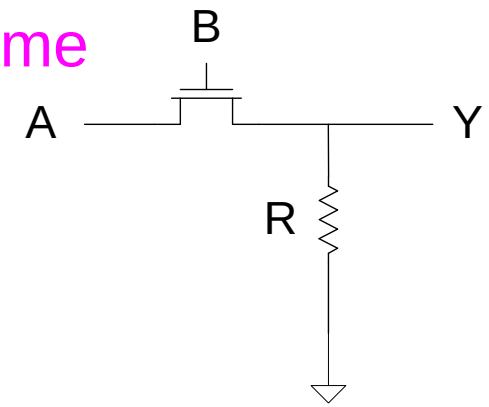
1. **PU network comprised of p-channel device**
2. **PD network comprised of n-channel device**
3. **One and only one of these networks is conducting at the same time**

Properties of PU/PD logic of this type (with simple switch-level model):

Rail to rail logic swings
Zero static power dissipation in both Y=1 and Y=0 states
Arbitrarily fast (too good to be true? will consider again with better model)

Pass Transistor Logic

Review from Last Time



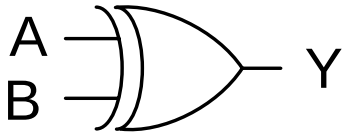
$$Y = A \bullet B$$

Requires only 1 transistor (and a resistor)

- **Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)**
- **Resistor may require more area than several hundred or even several thousand transistors**
- **Signal levels may not go to V_{DD} or to 0V**
- **Static power dissipation may not be zero**
- **Signals may degrade unacceptably if multiple gates are cascaded**
- **"resistor" often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist**
- **Pass transistor logic is widely used**

Review from Last Time

Example 2: XOR Function

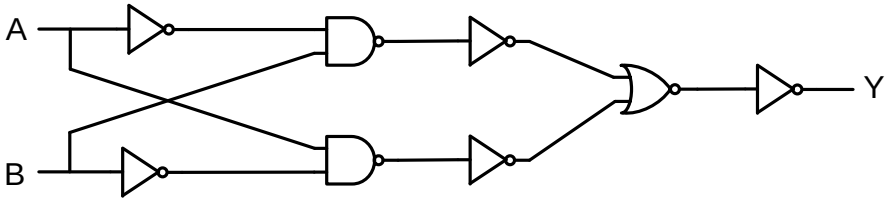


$$Y = A \oplus B$$

A widely-used 2-input Gate

Static CMOS implementation

$$Y = A\bar{B} + \bar{A}B$$

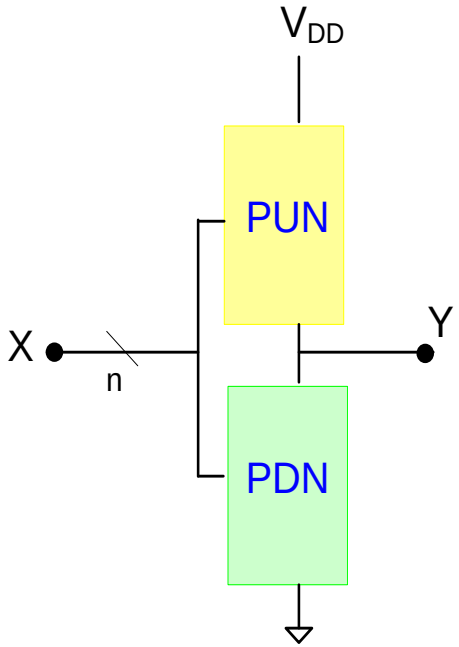


22 transistors 5 levels of logic

Delays unacceptable (will show later) and device count is too large !

Review from Last Time

Complex Gates



Complex Gate Design Strategy:

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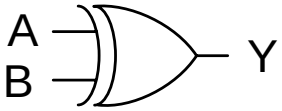
(Y and $\overline{Y}$ often expressed in either SOP or POS form)

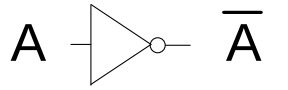
Review from Last Time

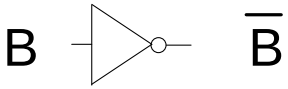
XOR in Complex Logic Gates

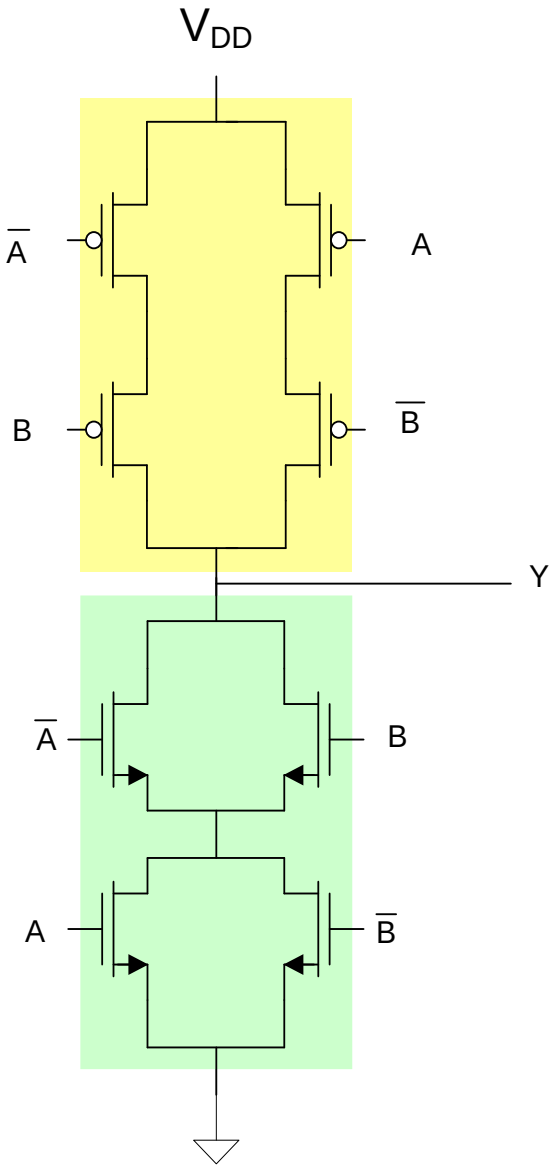


$$Y = A\bar{B} + \bar{A}B$$

$$\bar{Y} = (\bar{A}+B)\bullet(A+\bar{B})$$





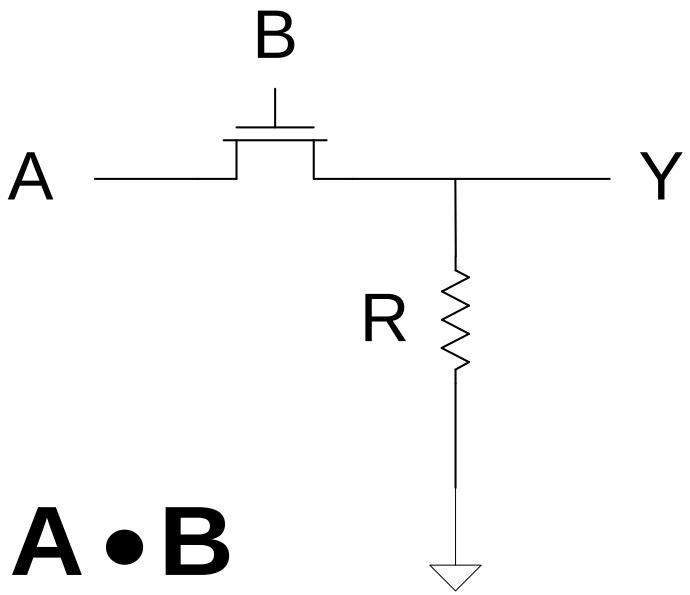


12 transistors and 2 levels of logic

Notice a significant reduction in the number of transistors required

Review from Last Time

Pass Transistor Logic



$$Y = A \bullet B$$

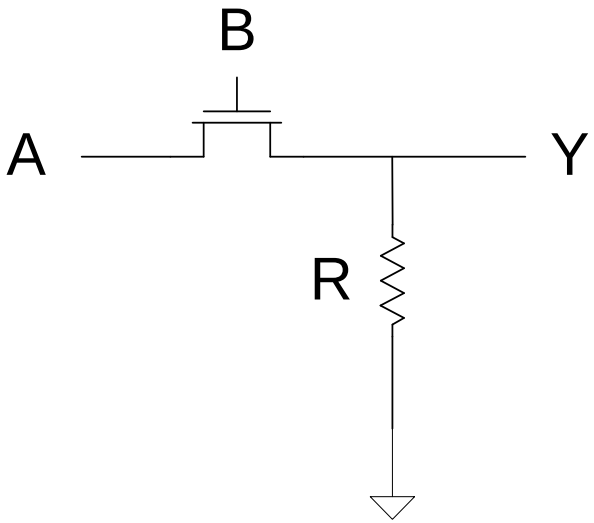
Even simpler pass transistor logic implementations are possible

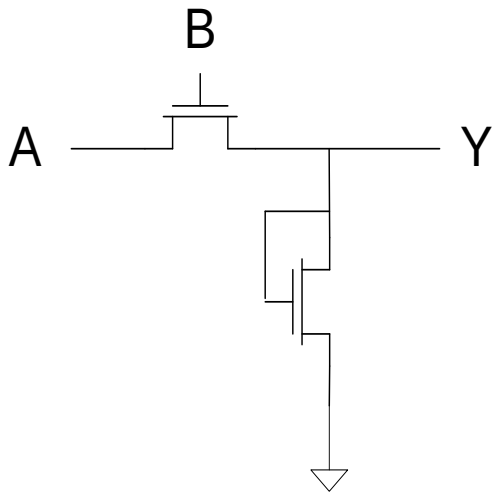
Requires only 1 transistor (and a resistor).

Will see later that the area of a single practical resistor for this circuit may be comparable to that needed for hundreds or even thousands of transistors

Review from Last Time

Pass Transistor Logic





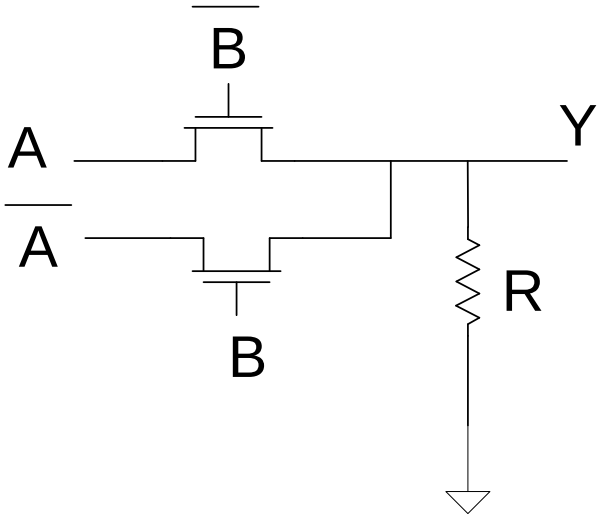
$$Y = A \bullet B$$

- **May be able to replace resistor with transistor (one of several ways shown)**
- **But high logic level can not be determined with existing device model (or even low logic level for circuit on right)**
- **Power dissipation can not be determined with existing device model for circuit on right**

Better device model is needed (Power? Signal Swing? Speed?)

Review from Last Time

Pass Transistor Logic



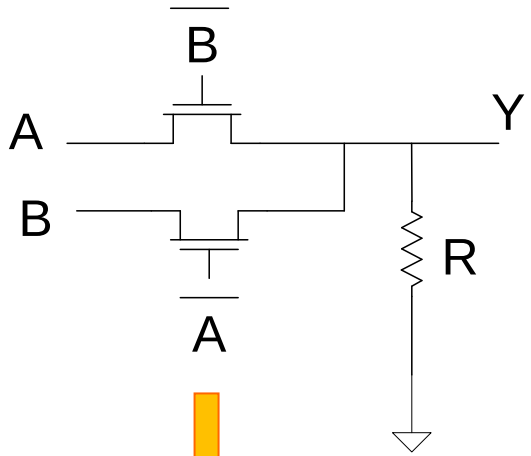
$$Y = A \oplus B$$

6 transistors, 1 resistor, two levels of logic

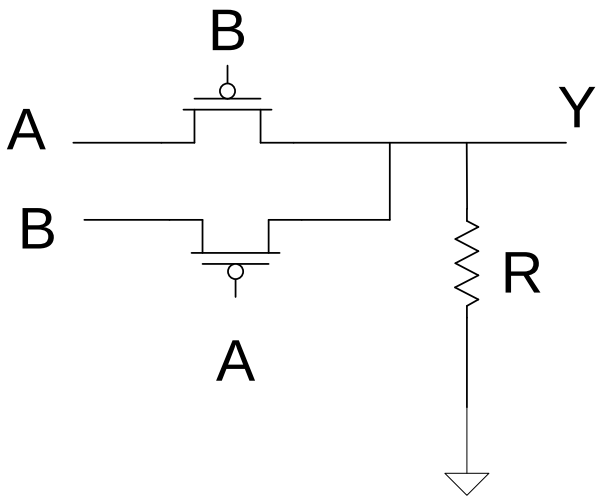
(the 4 transistors in the two inverters are not shown)

Review from Last Time

Pass Transistor Logic



$$Y = A \oplus B$$

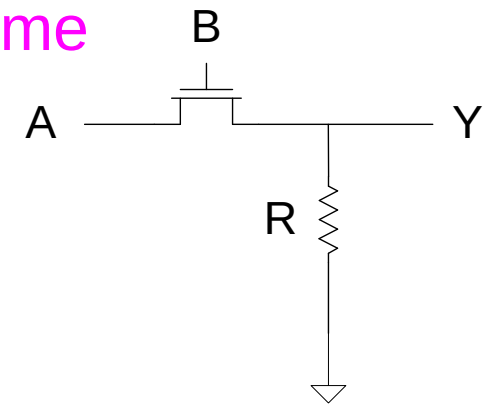


$$Y = A \oplus B$$

2 transistors, 1 resistor, one level of logic

Pass Transistor Logic

Review from Last Time



$$Y = A \bullet B$$

Requires only 1 transistor (and a resistor)

- **Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)**
- **Resistor may require more area than several hundred or even several thousand transistors**
- **Signal levels may not go to V_{DD} or to 0V**
- **Static power dissipation may not be zero**
- **Signals may degrade unacceptably if multiple gates are cascaded**
- **"resistor" often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist**
- **Pass transistor logic is widely used**

Review from Last Time

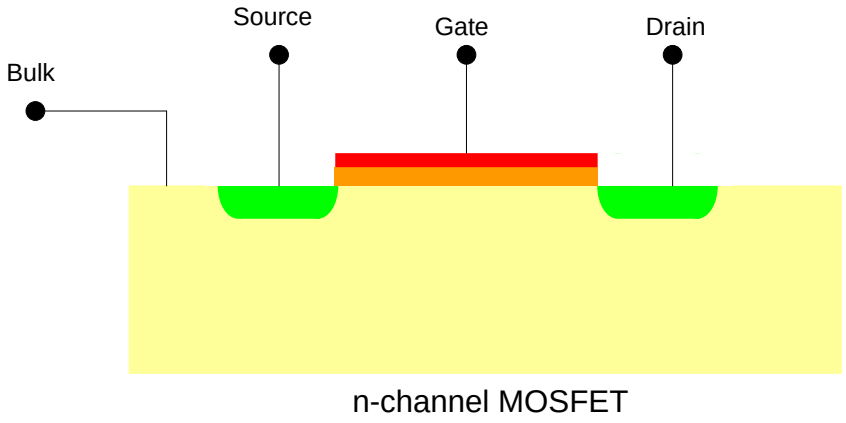
Logic Design Styles

- Several different logic design styles are often used throughout a given design (3 considered thus far)
  - Static CMOS
  - Complex Logic Gates
  - Pass Transistor Logic
- The designer has complete control over what is placed on silicon and governed only by cost and performance
- New logic design strategies have been proposed recently and others will likely emerge in the future
- The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements

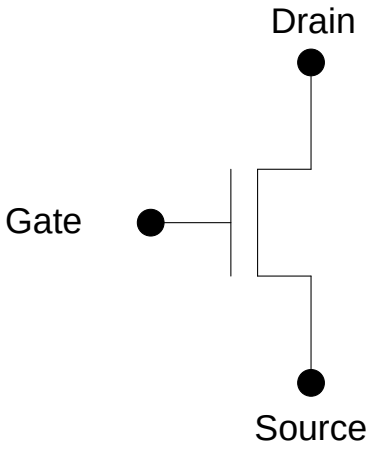
Review from Last Time

MOS Transistor

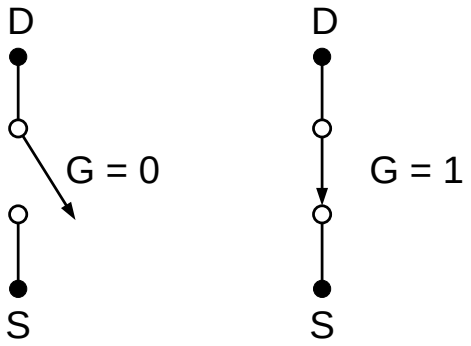
Qualitative Discussion of n-channel Operation



n-channel MOSFET



Equivalent Circuit for n-channel MOSFET



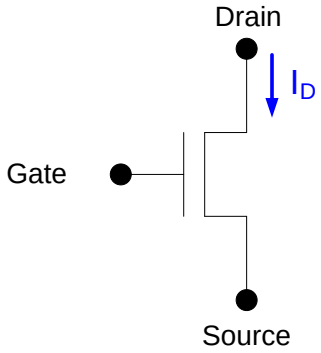
- **Source assumed connected to (or close to) ground**
- **V_{GS}=0 denoted as Boolean gate voltage G=0**
- **V_{GS}=V_{DD} denoted as Boolean gate voltage G=1**
- **Boolean G is relative to ground potential**

This is the first model we have for the n-channel MOSFET !

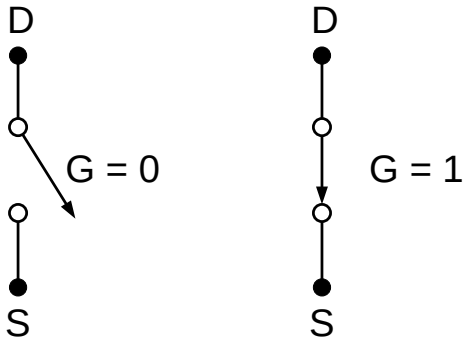
Ideal switch-level model

Review from Last Time

MOS Transistor MODEL



Equivalent Circuit for n-channel MOSFET with source as ground

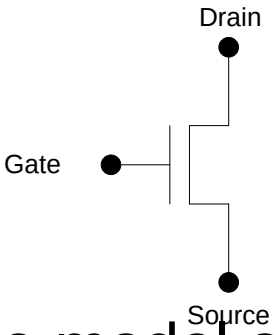


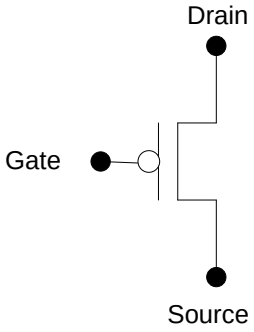
Mathematical model (not dependent upon Boolean notation):

$I_D = 0$	if V_{GS} is low (or negative)
$V_{DS} = 0$	if V_{GS} is high

- Pass Transistor Logic
- Improved Switch-Level Model
- Propagation Delay
- Stick Diagrams
- Technology Files

MOSFET Modeling

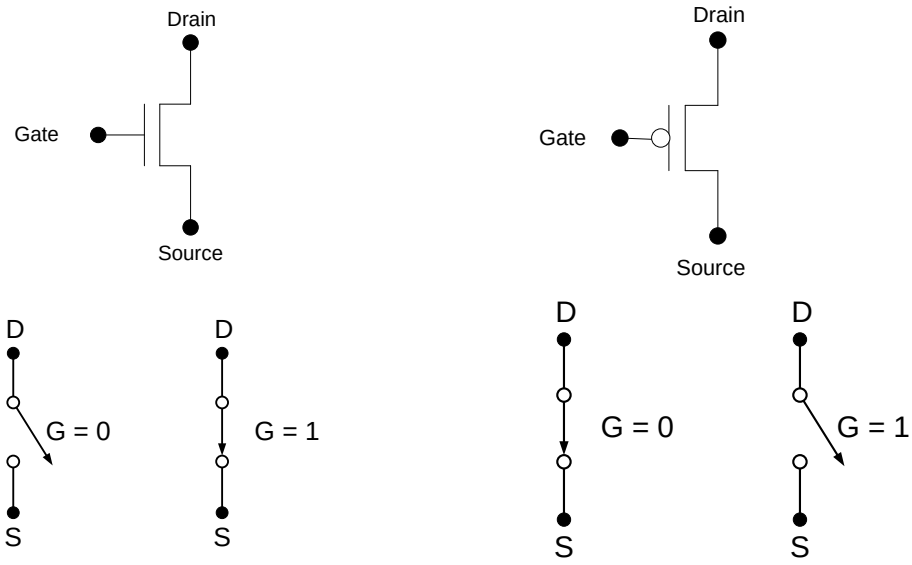




- Simple model of MOSFET was developed (termed switch-level model)
- Simple gates designed in CMOS Process were introduced
  - Some have zero power dissipation
  - Some have or appeared to have rail to rail logic voltage swings
  - All appeared to be Infinitely fast
  - Logic levels of some can not be predicted with simple model
  - Simple model is not sufficiently accurate to provide insight relating to some of these properties
- MOSFET modeling strategy
  - hierarchical model structure will be developed
  - generally use simplest model that can be justified

MOS Transistor Models

1, Switch-Level model



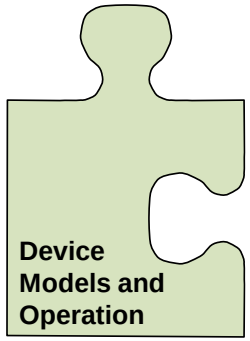
Advantages:

Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

Limitations:

Does not provide timing information (surfaced when looking at static CMOS circuits, and several others that have not yet become apparent from the applications that have been considered) and can not support design of "resistor" used in Pass Transistor Logic

Improved Device Models



With the simple switch-level model, it was observed that basic static CMOS logic gates have the following three properties:

- **Rail to rail logic swings**
- **Zero static power dissipation in both Y=1 and Y=0 states**
- **Arbitrarily fast (too good to be true? will consider again with better model)**

It can be shown that the first two properties are nearly satisfied in actual fabricated circuits with p-channel/n-channel PU/PD logic but though the circuits are fast, they are observably not arbitrarily fast

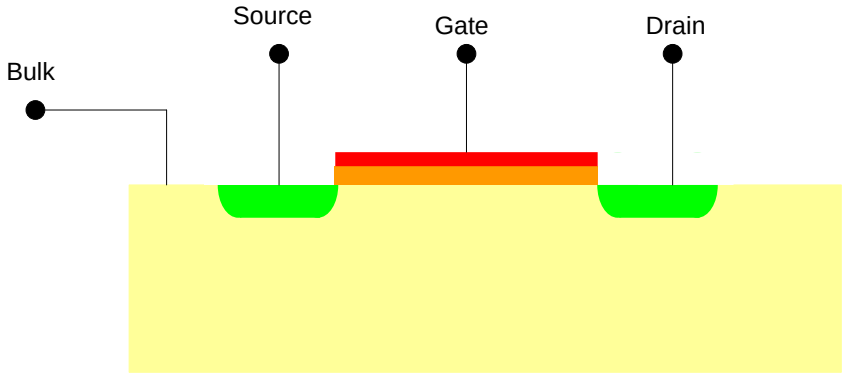
None of these properties are observed for some logic styles such as Pass Transistor Logic

Will now extend switch-level model to predict speed of basic gates in static CMOS and logic levels and power dissipation in PTL

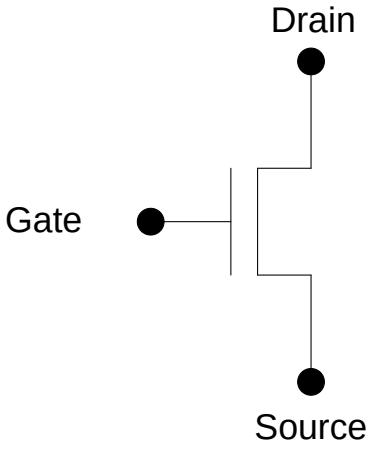
Recall

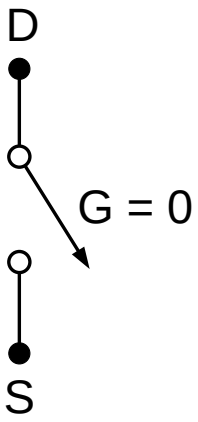
MOS Transistor

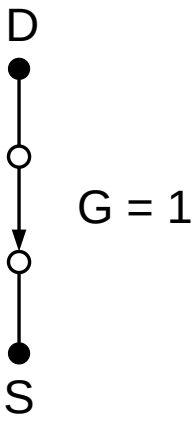
Qualitative Discussion of n-channel Operation



n-channel MOSFET



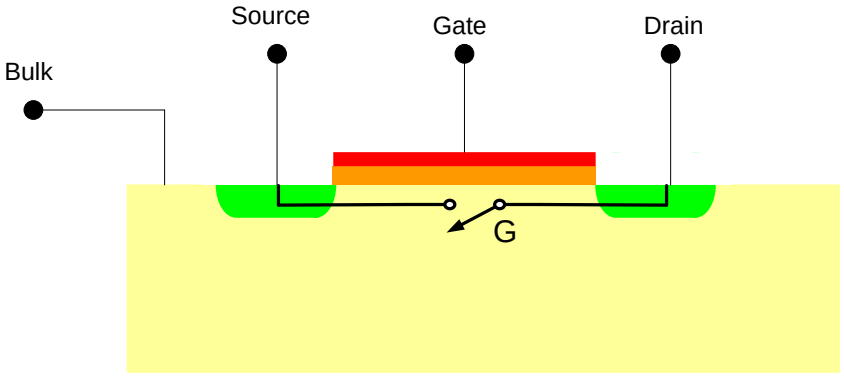




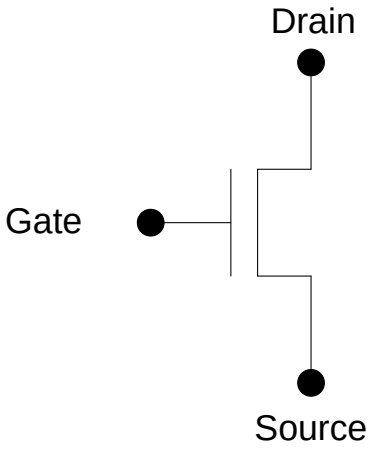
This was the first model introduced and was termed the basic switch-level mode

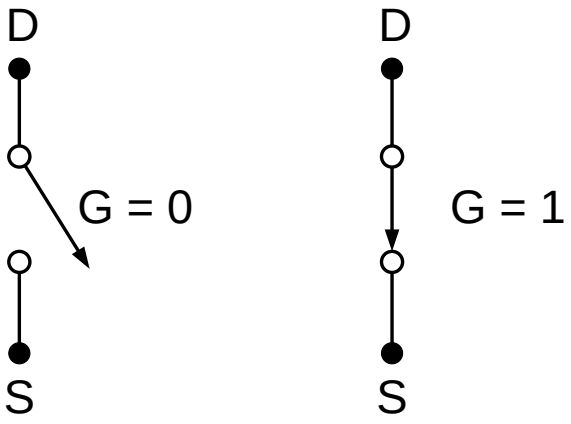
MOS Transistor

Qualitative Discussion of n-channel Operation



n-channel MOSFET

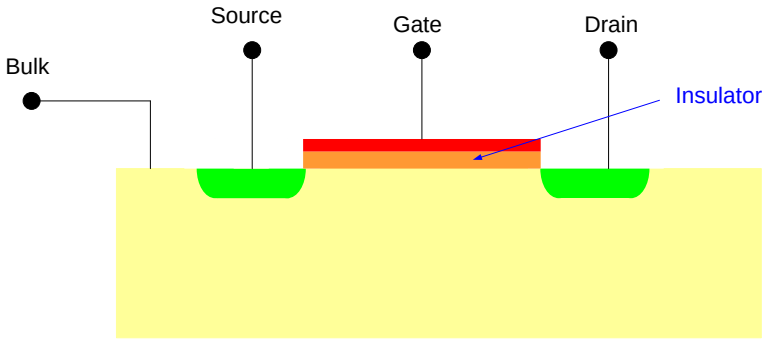




Conceptual view of basic switch-level model

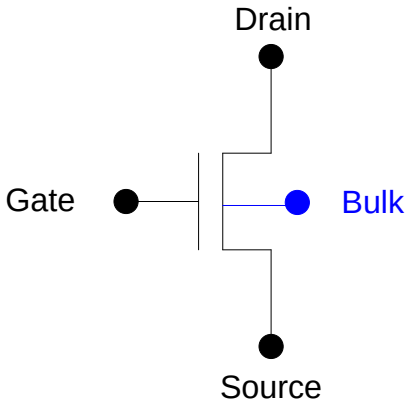
MOS Transistor

Qualitative Discussion of n-channel Operation

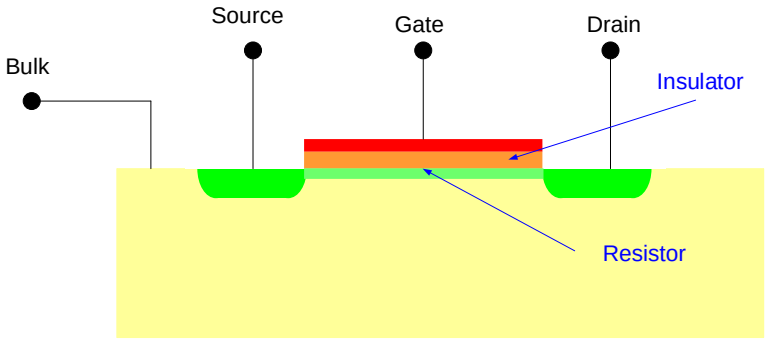


n-channel MOSFET

For V_{GS} small



MOSFET actually 4-terminal device



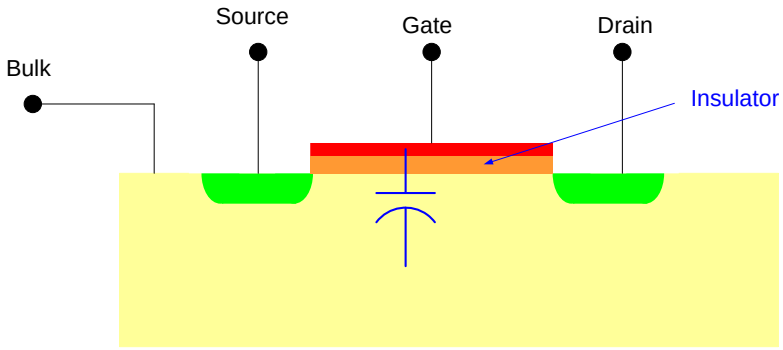
n-channel MOSFET

For V_{GS} large

- Region under gate termed the “channel”
- When “resistor” is electrically created, region where it resides in channel is termed an “inversion region”

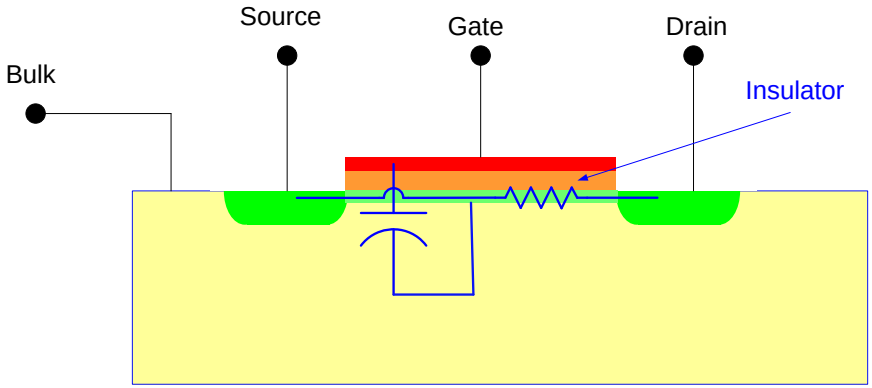
MOS Transistor

Qualitative Discussion of n-channel Operation



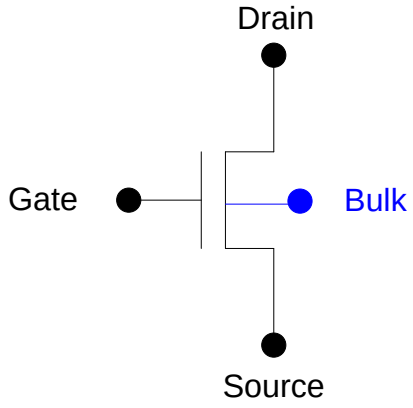
n-channel MOSFET

For V_{GS} small



n-channel MOSFET

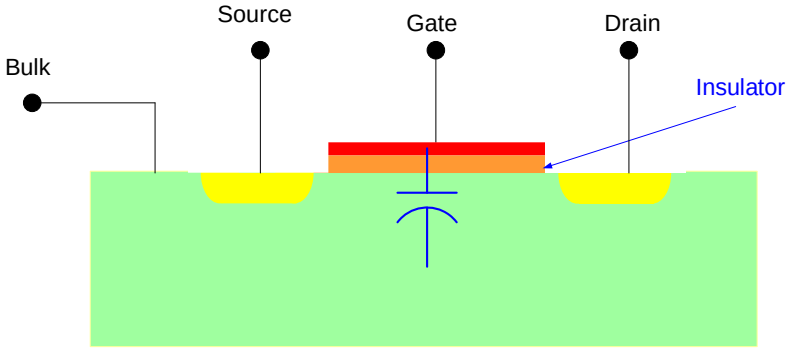
For V_{GS} large



- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

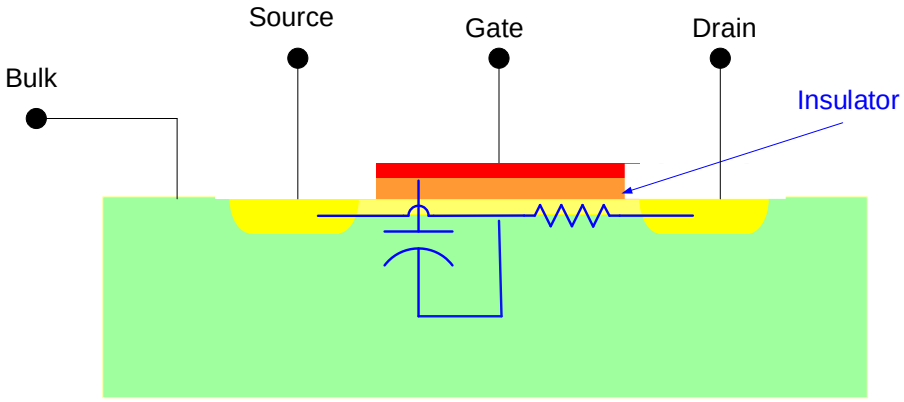
MOS Transistor

Qualitative Discussion of p-channel Operation

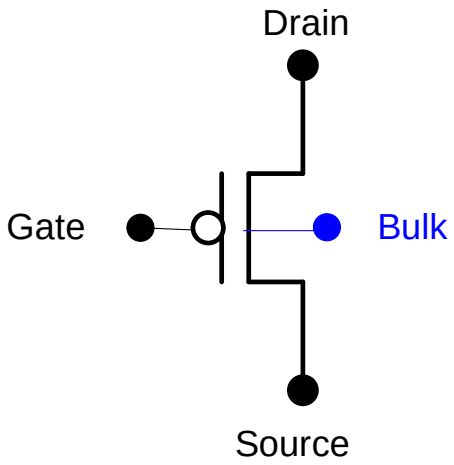


p-channel MOSFET

For $|V_{GS}|$ small



p-channel MOSFET



For $|V_{GS}|$ large

- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
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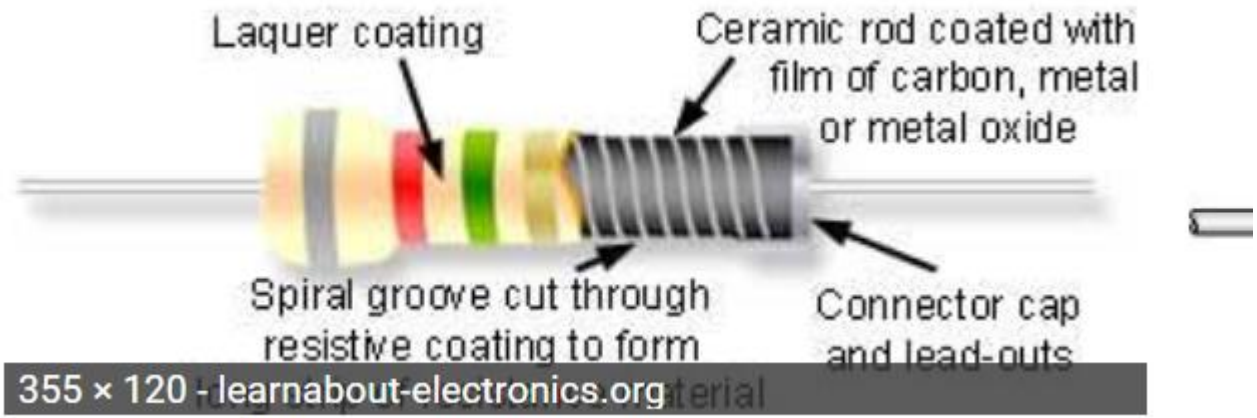
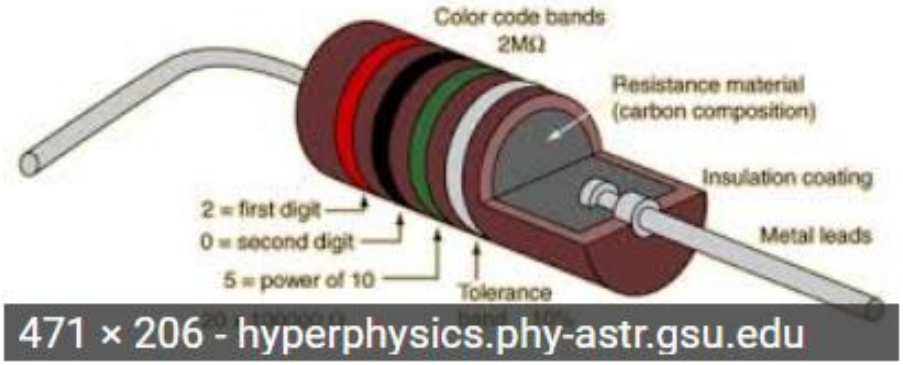
Discrete Resistors often use thin films too though not electrically created

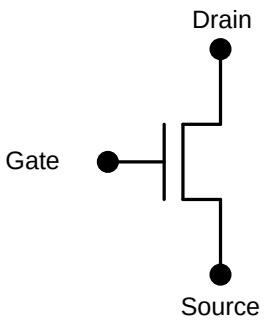
- **Thin-film spiral wound**

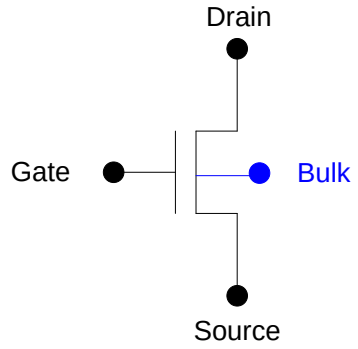


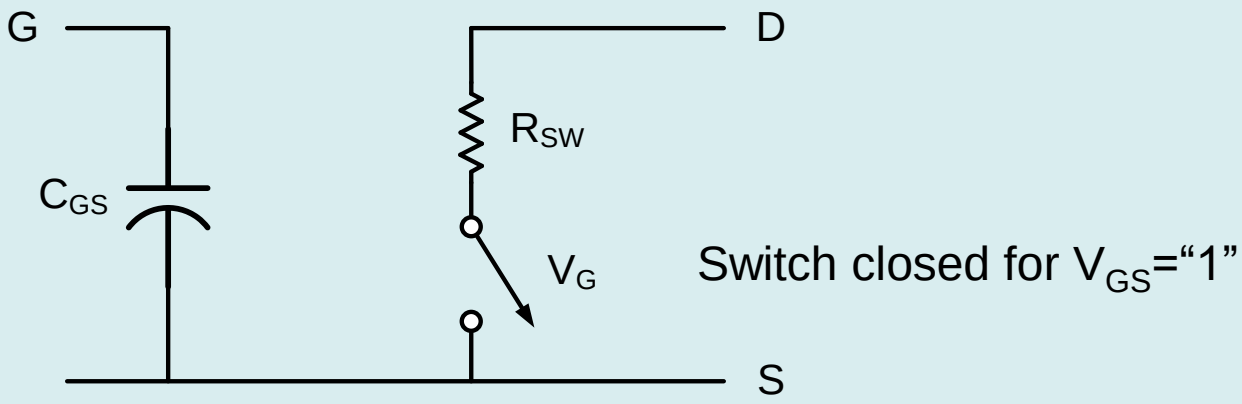
- **Carbon composition**



Improved Switch-Level Model



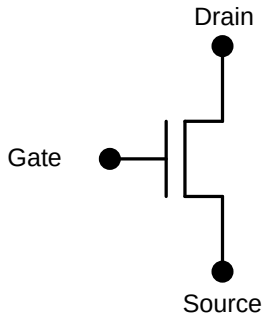




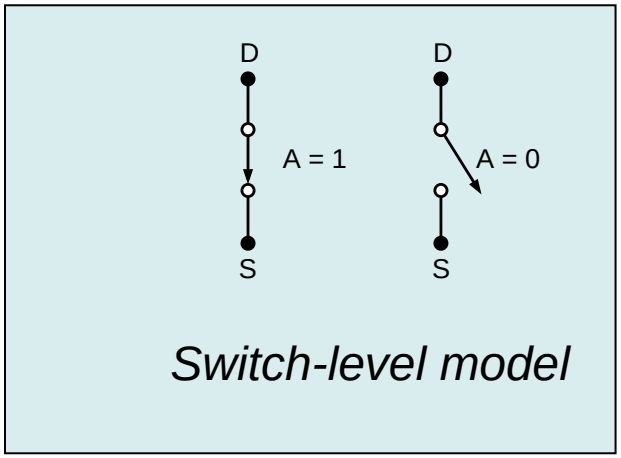
Switch-level model including gate capacitance and channel resistance

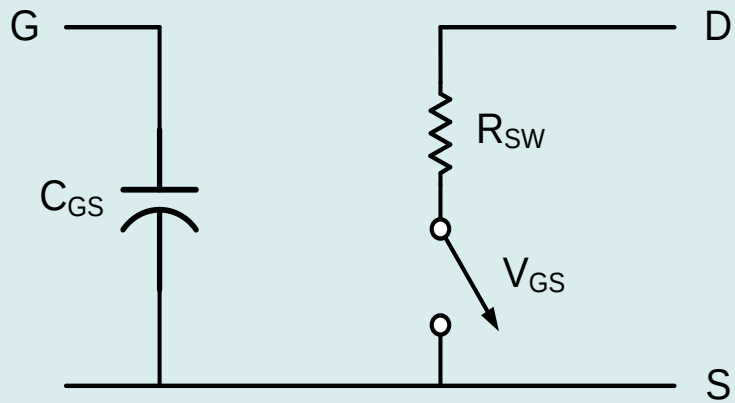
- Connect the gate capacitance to the source to create lumped model
- Still neglect bulk connection

Improved Switch-Level Model



n-channel





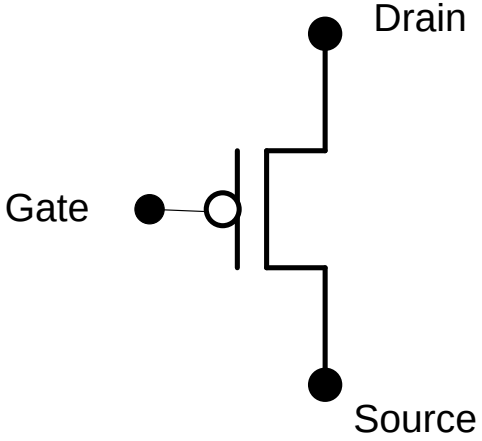
Switch closed for V_{GS}= large

Alt: switch closed for "A = 1"

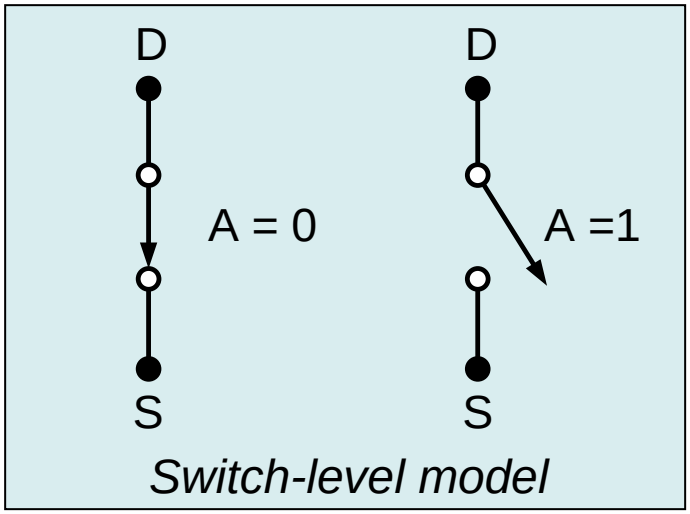
A denotes Boolean signal on Gate

Switch-level model including gate capacitance and channel resistance

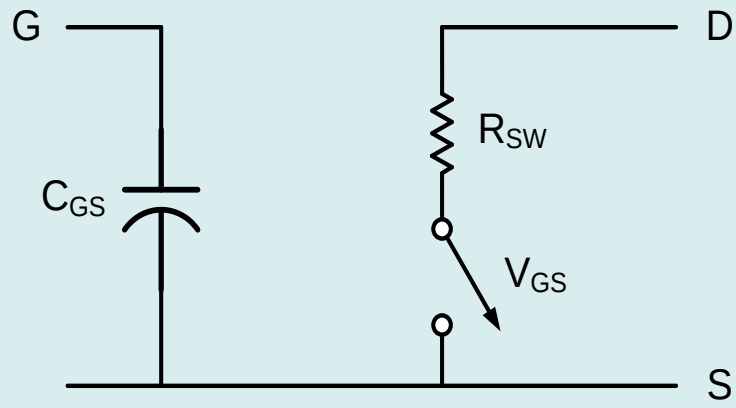
Improved Switch-Level Model



p-channel



Switch-level model



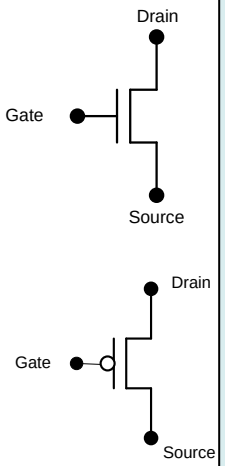
Switch closed for $|V_{GS}|$ large

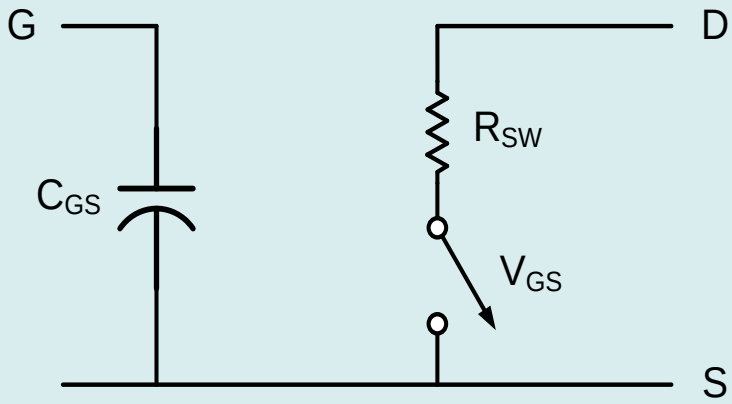
Alt: If S near V_{DD}, closed for A=0

A denotes Boolean signal on Gate

Switch-level model including gate capacitance and channel resistance

Improved Switch-Level Model





Switch closed for A =1 , n-ch
Switch closed for A =0 , p-ch

A denotes Boolean signal on Gate

Switch-level model including gate capacitance and channel resistance

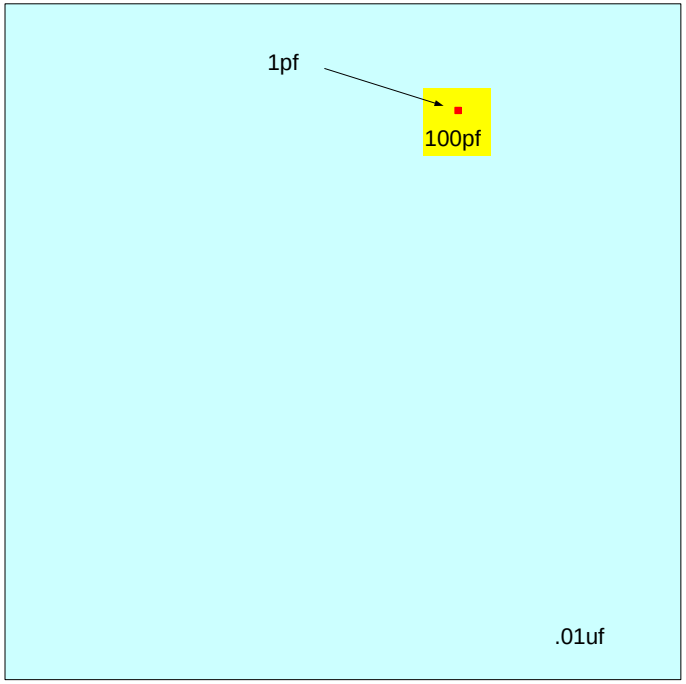
C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process with V_{DD}=5V

$$\mathbf{C_{GS} \cong 1.5fF} \qquad \mathbf{R_{sw}} \cong \begin{cases} \mathbf{2K\Omega \ \ n-channel} \\ \mathbf{6K\Omega \ \ p-channel} \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Is a capacitor of 1.5fF small enough to be neglected?

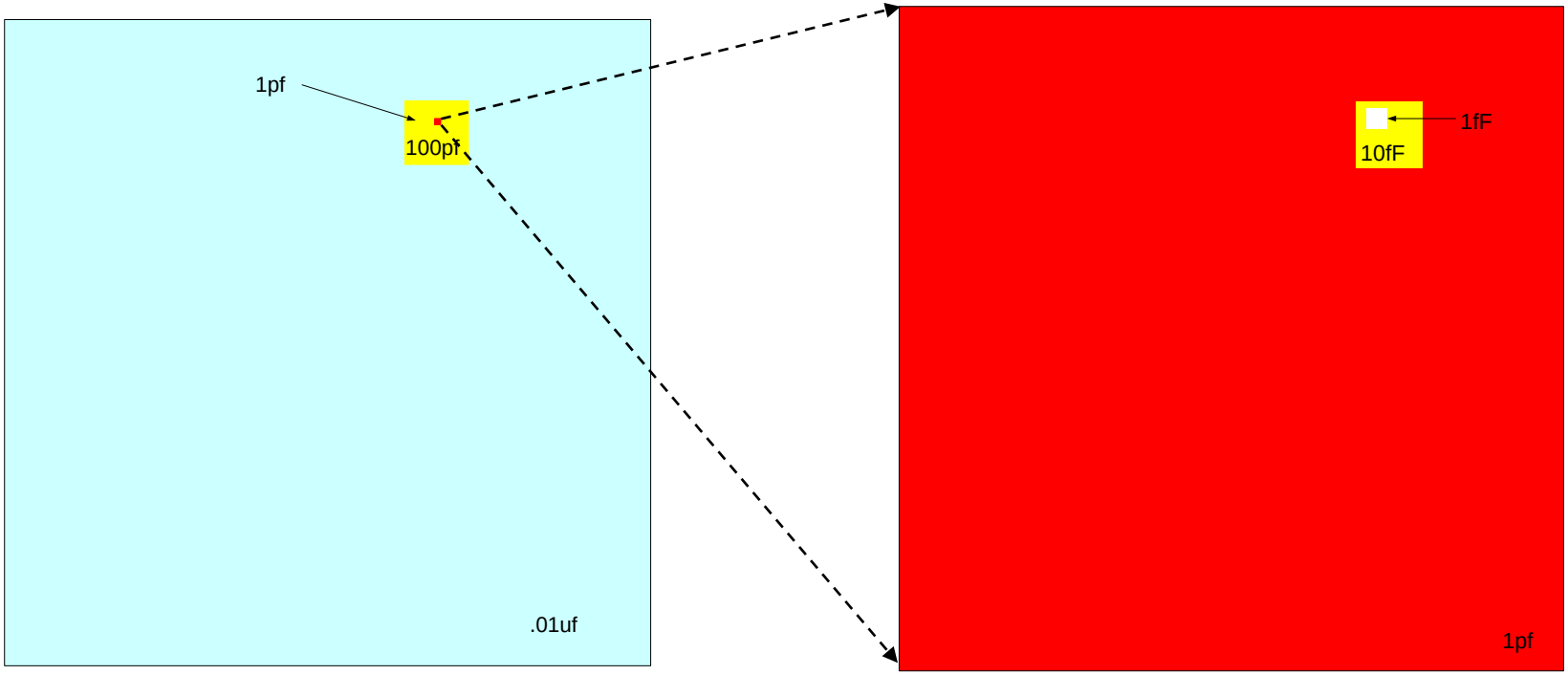


From EE 201 Parts Kit

Capacitors (Farads)		
100p	3	
470p	3	
0.001u	3	2
0.0047u	3	2
0.01u	3	
0.047u	3	
0.1u	3	1
0.47u	3	
1u	3	
10u	3	
100u	3	

Area allocations shown to relative scale:

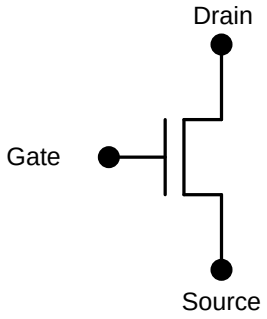
Is a capacitor of 1.5fF small enough to be neglected?



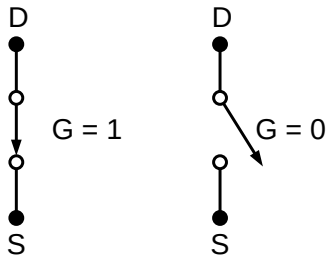
Area allocations shown to relative scale:

- **Not enough information at this point to determine whether this very small capacitance can be neglected**
- **Will answer this important question later**

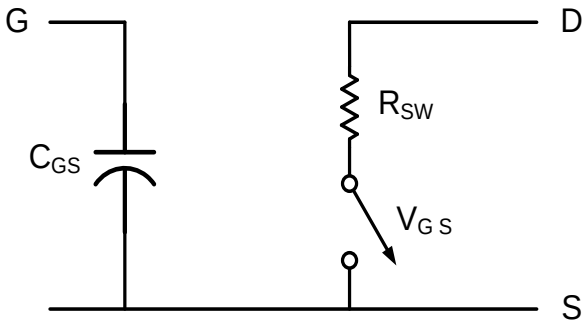
Model Summary (for n-channel)



1. Switch-Level model



2. Improved switch-level model

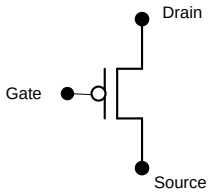


Switch closed for V_{GS}= large

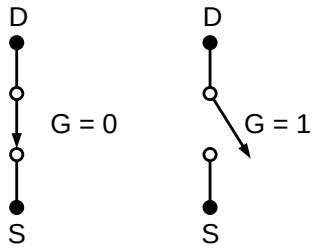
Switch open for V_{GS}= small

Other models will be developed later

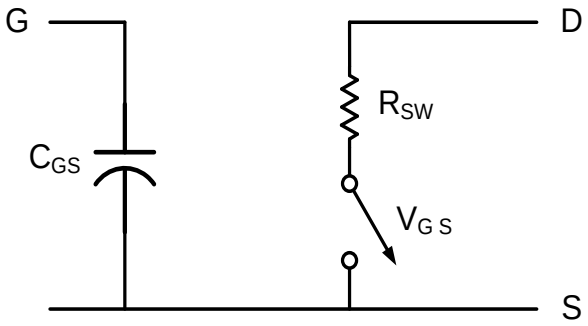
Model Summary (for p-channel)



1. Switch-Level model



2. Improved switch-level model



Switch closed for $|V_{GS}|$= large

Switch open for $|V_{GS}|$= small

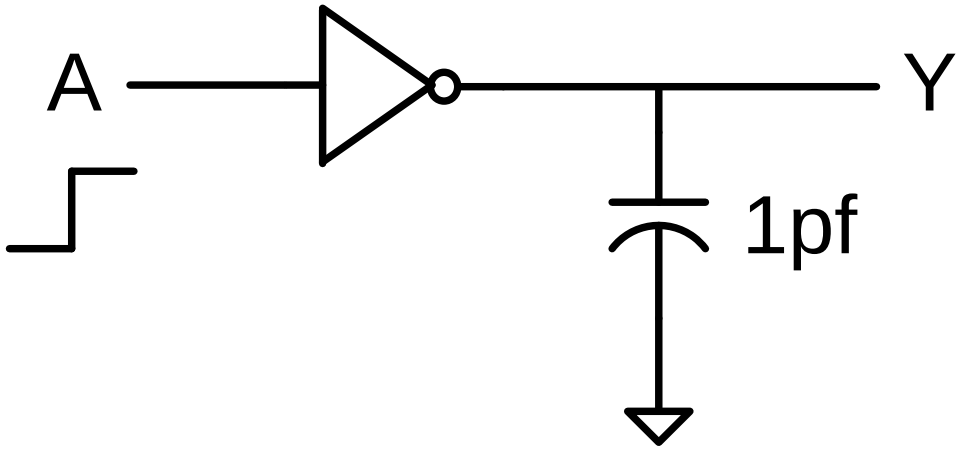
Other models will be developed later

- Pass Transistor Logic
- Improved Switch-Level Model
- Propagation Delay
- Stick Diagrams
- Technology Files

Example

What are t_{HL} and t_{LH}?

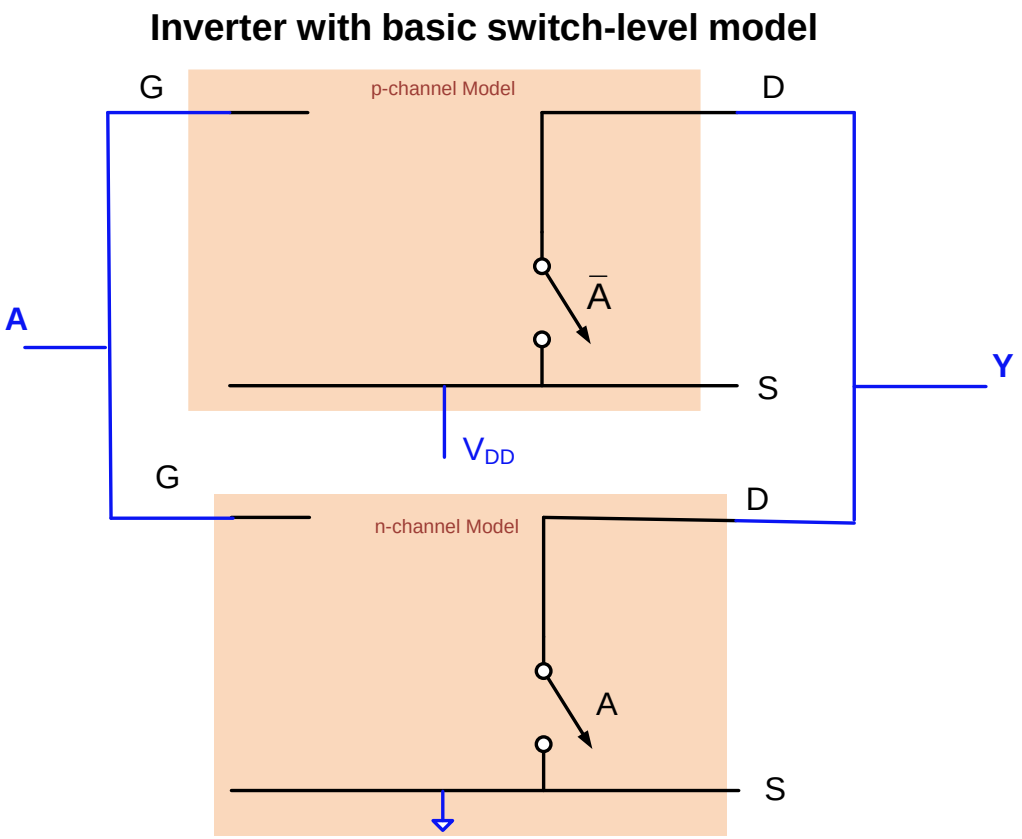
Assume V_{DD}=5V



With basic switch level model ?

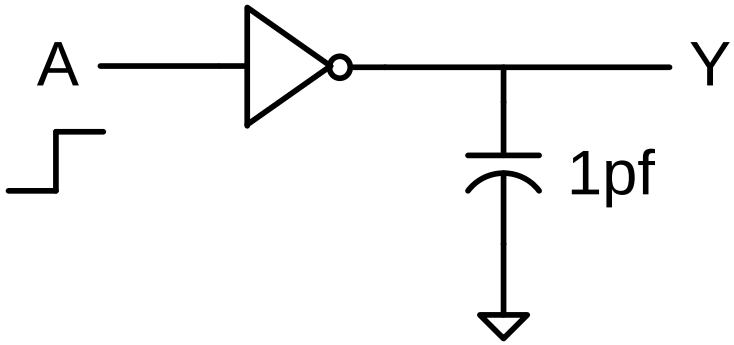
With improved switch level model ?

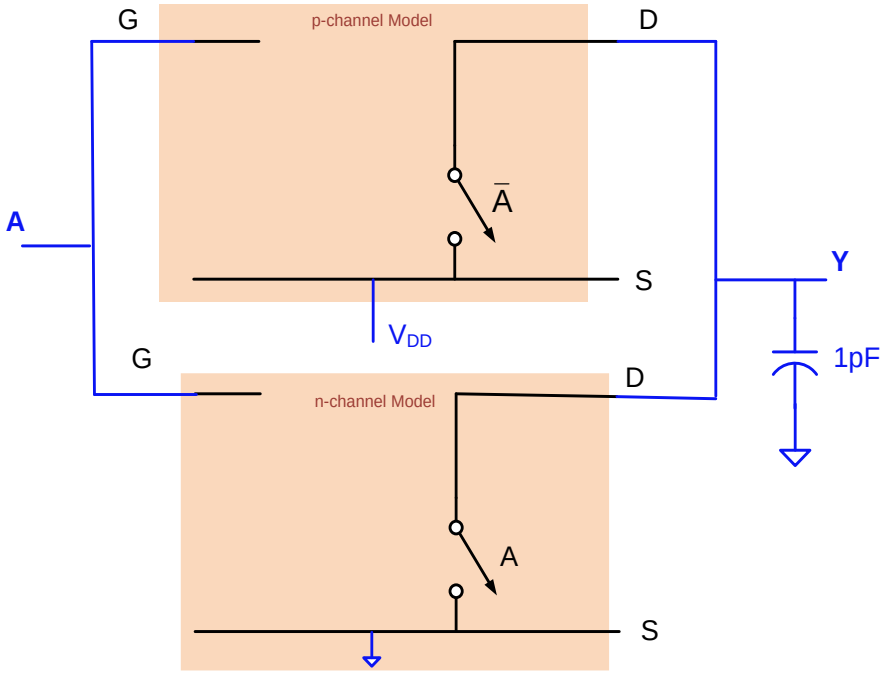
Example


Inverter with basic switch-level model
G
p-channel Model
D
$\overline{A}$
A
S
Y
V_{DD}
G
D
n-channel Model
A
S

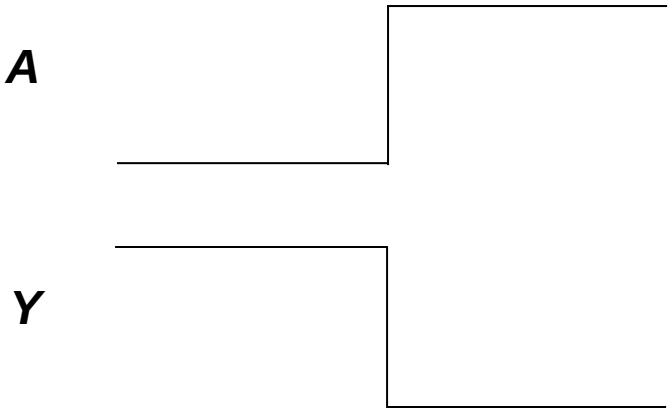
Example

What are t_{HL} and t_{LH}?





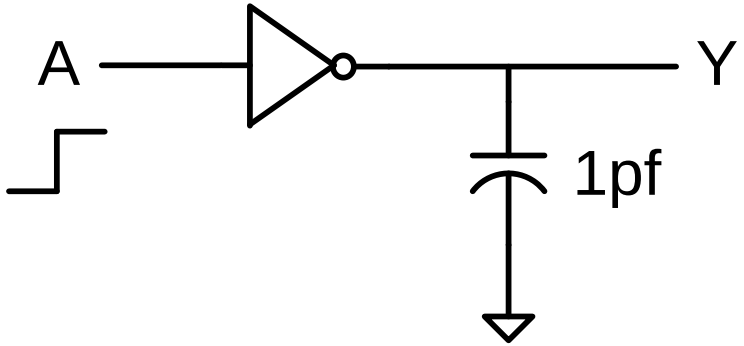
With basic switch level model



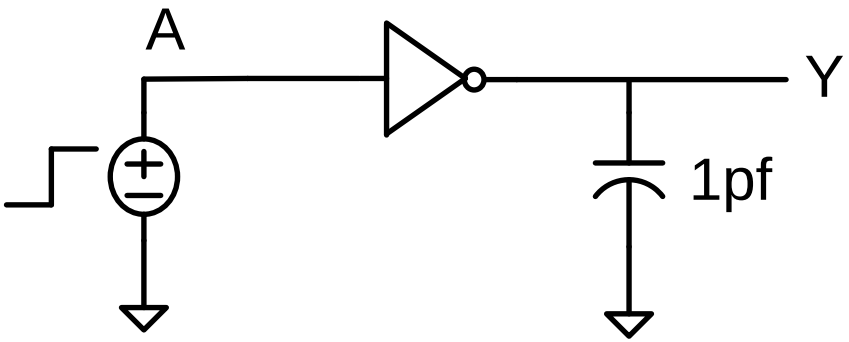
$t_{HL}=t_{LH}=0$

Example (cont)

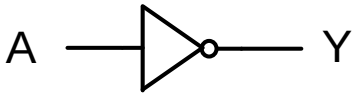
With simple switch-level model $t_{HL}=t_{LH}=0$



With improved model ?



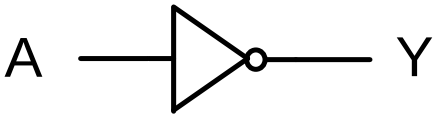
Inverter Model?



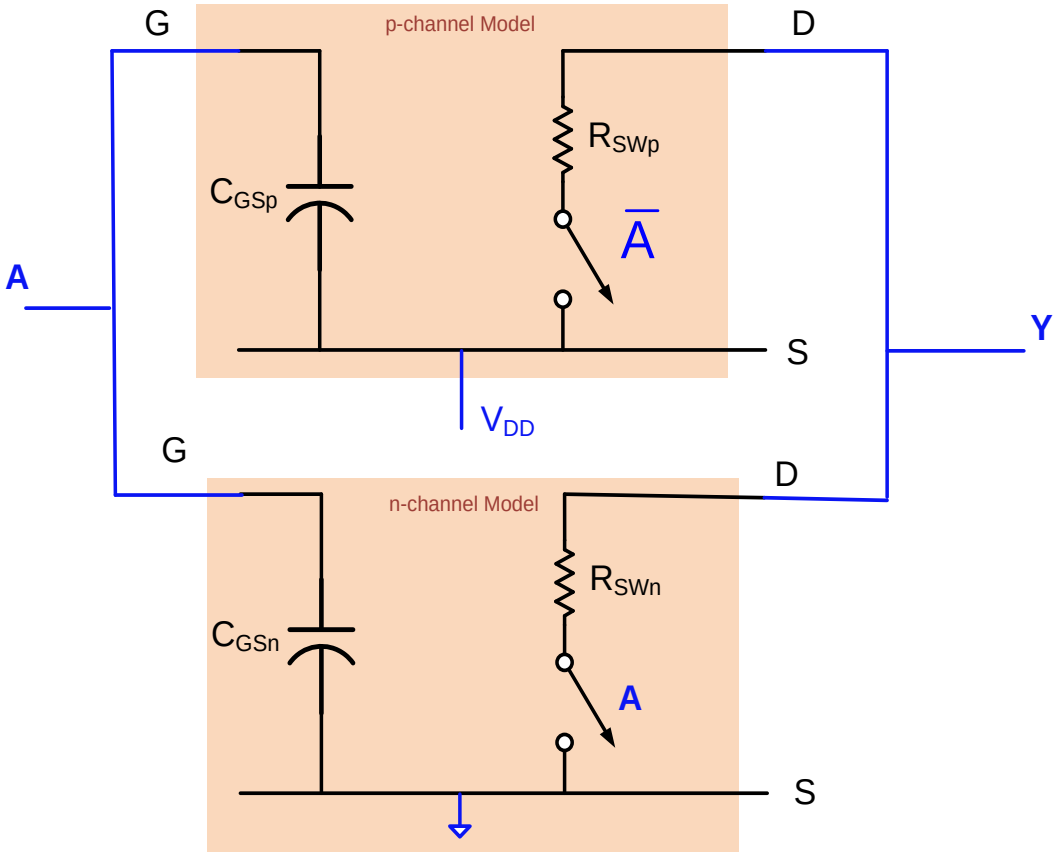
Example (cont)

Inverter with improved model

Inverter Model

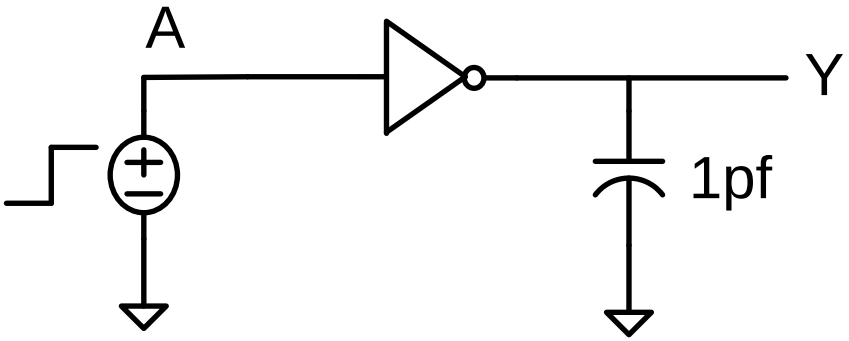


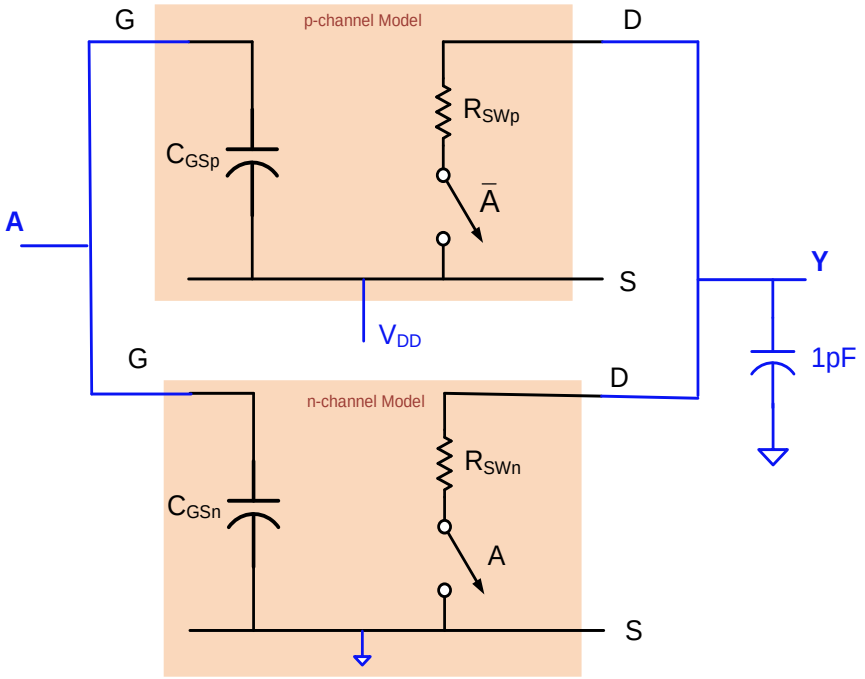
Inverter with Improved Model



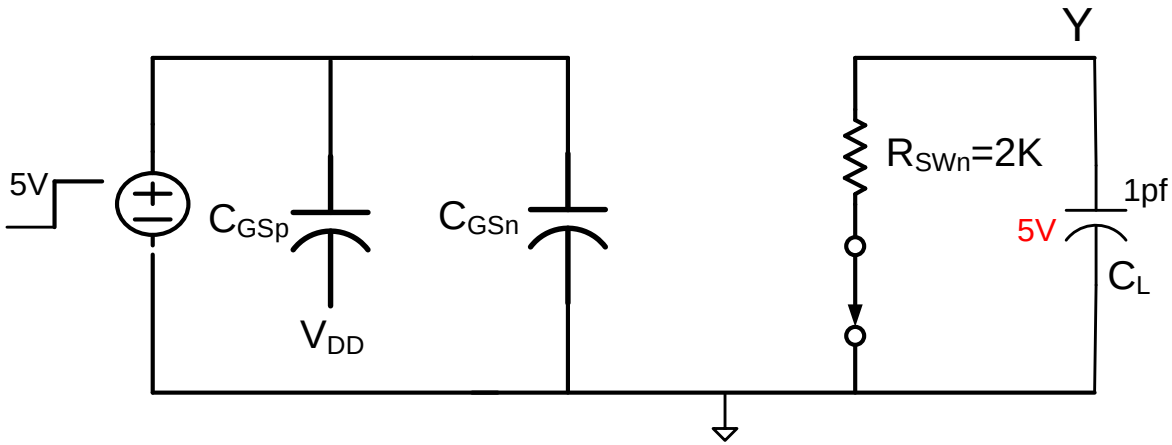
Example (cont)

With improved model $t_{HL}=?$





To initiate a HL output transisition, assume Y has been in the high state for a long time and lower switch closes at time t=0

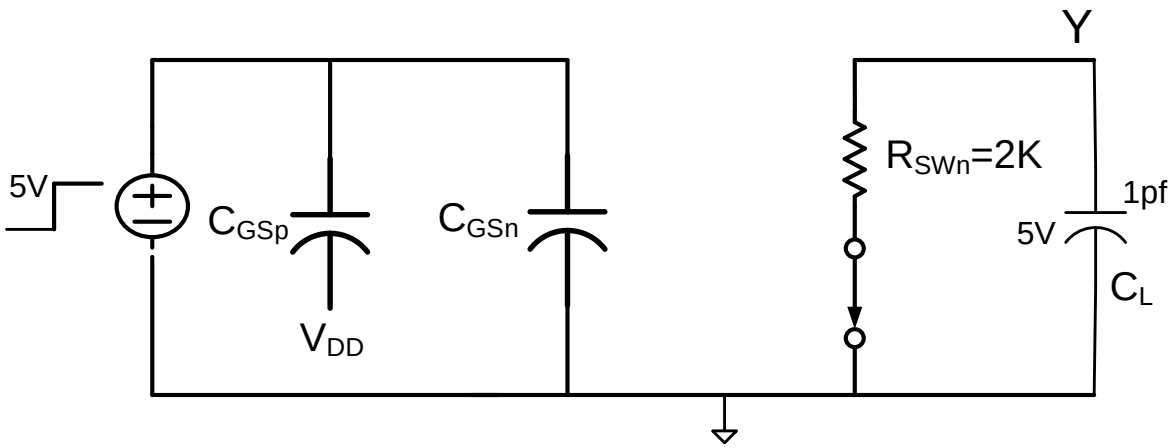


5V is the initial condition on C_L

Example (cont)

With improved model

t_{HL}=?



Recognize circuit as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

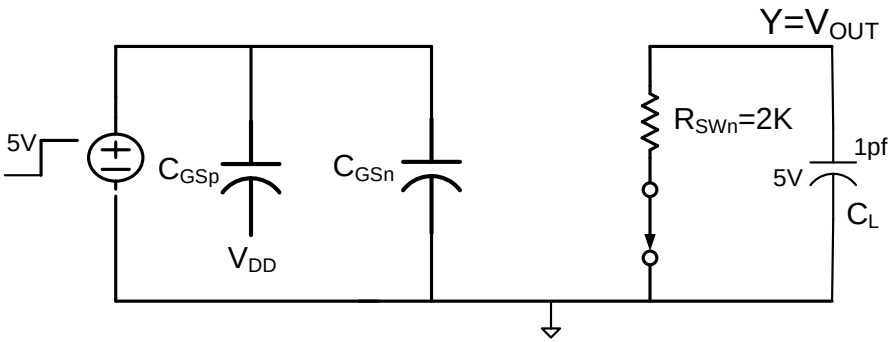
where F is the final value, I is the initial value and τ is the time constant of the circuit

(from Chapter 7 of Nilsson and Riedel)

For the circuit above, F=0, I=5 and $\tau = R_{SWn}C_L$

Example (cont)

With improved model

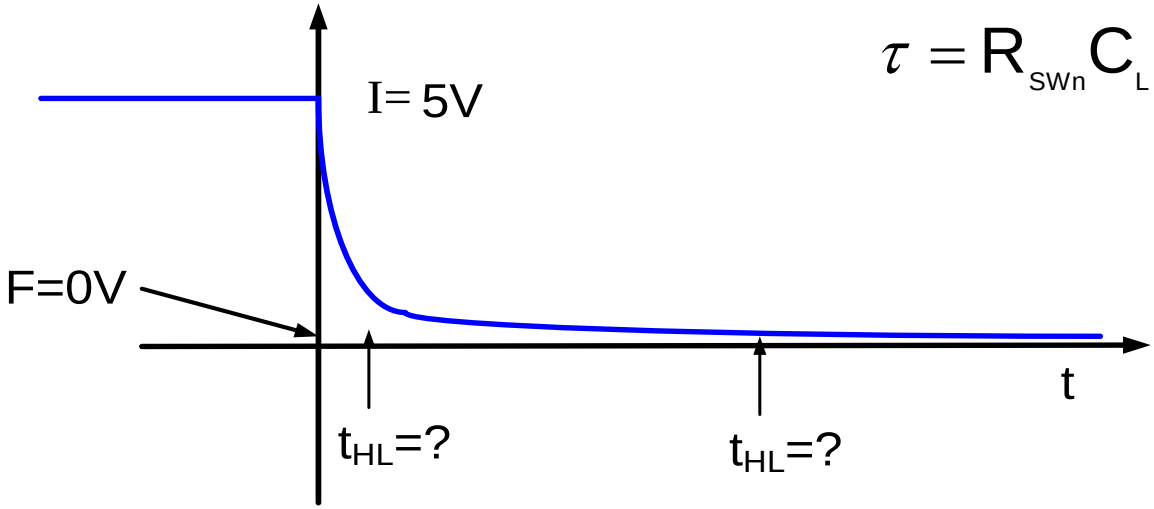


$t_{HL}=?$

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 5e^{-\frac{t}{\tau}}$$

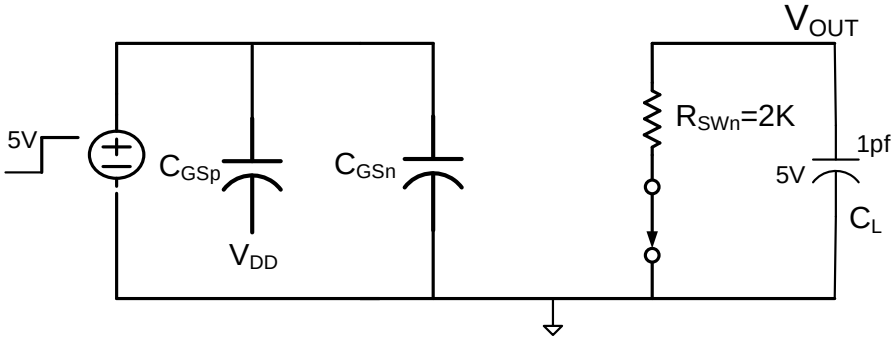
$$\tau = R_{SWn}C_L$$

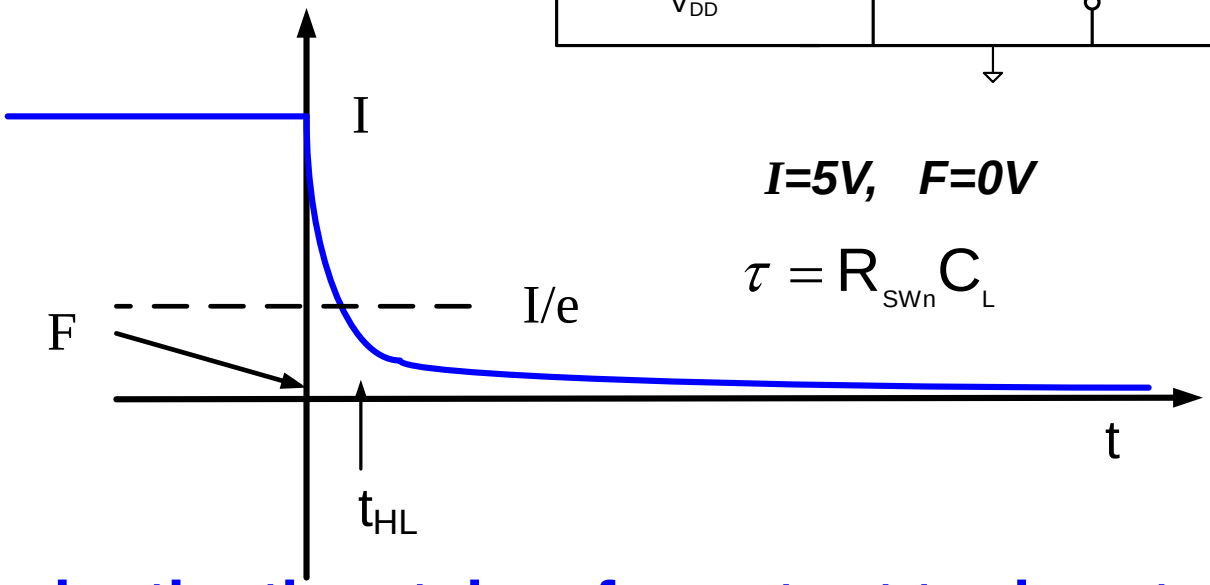


how is t_{HL} defined?

Example (cont)

t_{HL}=?





I=5V, F=0V

$$\tau = R_{SWn} C_L$$

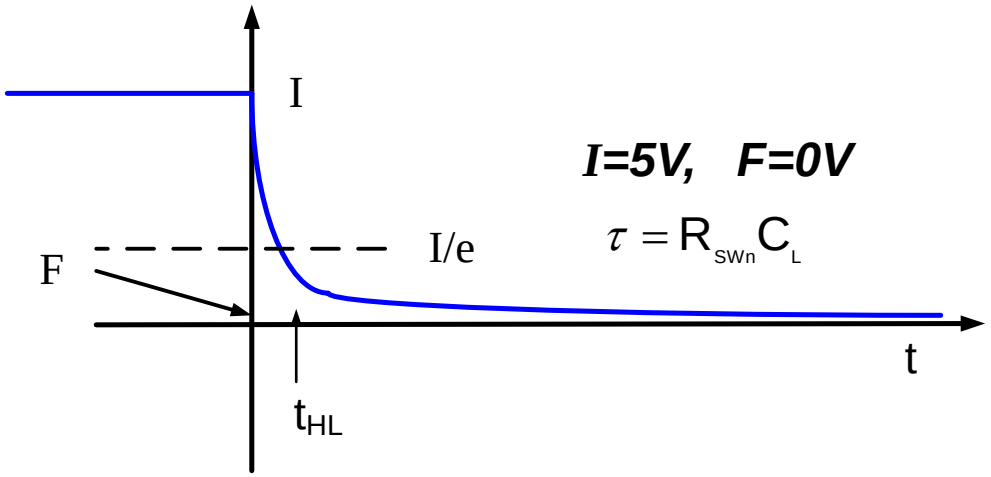
Define t_{HL} to be the time taken for output to drop to I/e

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \quad \Rightarrow \quad \frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}$$

t_{HL} as defined here has proven useful at analytically predicting response time of circuits

Example (cont)

With improved model



$$\frac{I}{e} = F + (I - F)e^{-\frac{t_{HL}}{\tau}}$$

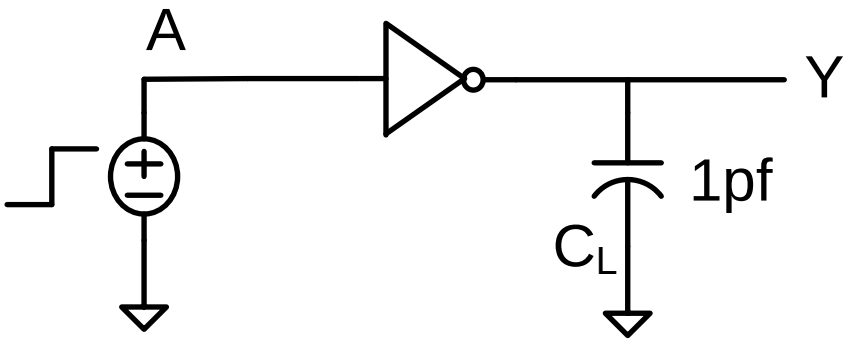
$$\frac{I}{e} = Ie^{-\frac{t_{HL}}{\tau}}$$

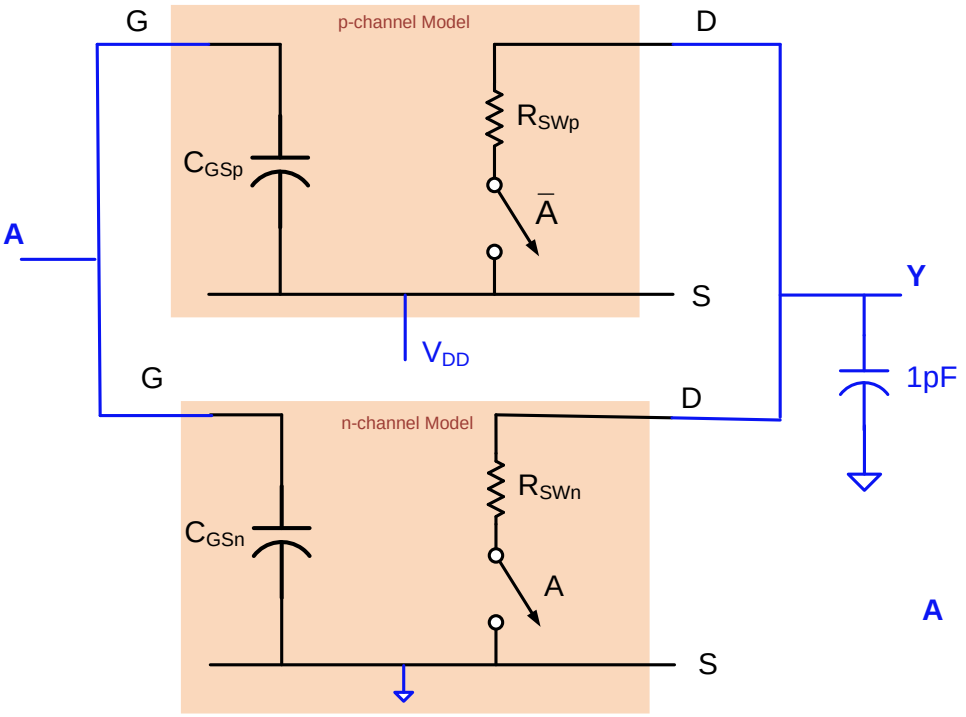
$$\frac{1}{e} = e^{-\frac{t_{HL}}{\tau}}$$

$$t_{HL} = \tau \quad \Rightarrow \quad t_{HL} = R_{SWn} C_L$$

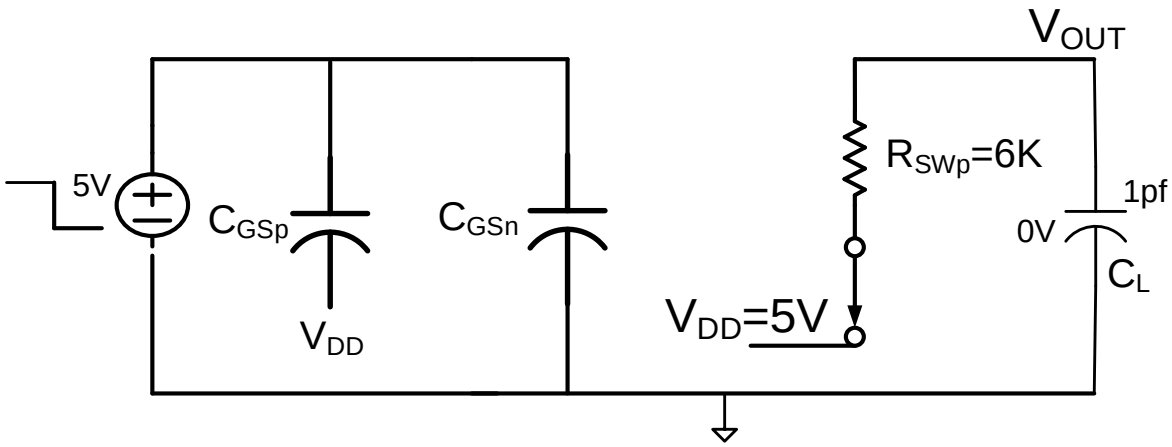
Example (cont)

With improved model $t_{LH}=?$





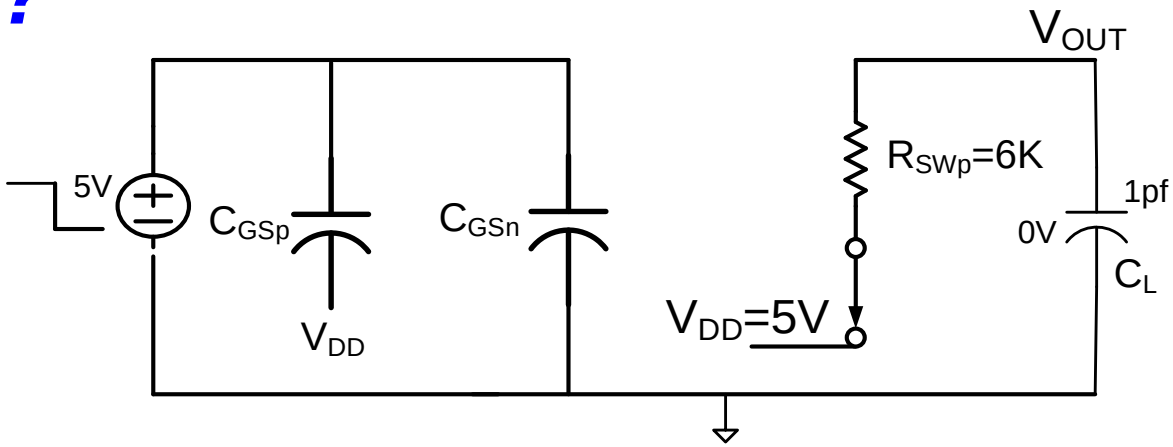
Assume output in low state for a long time and upper switch closes at time t=0



0V is the initial condition on C_L

Example (cont)

With improved model $t_{LH}=?$

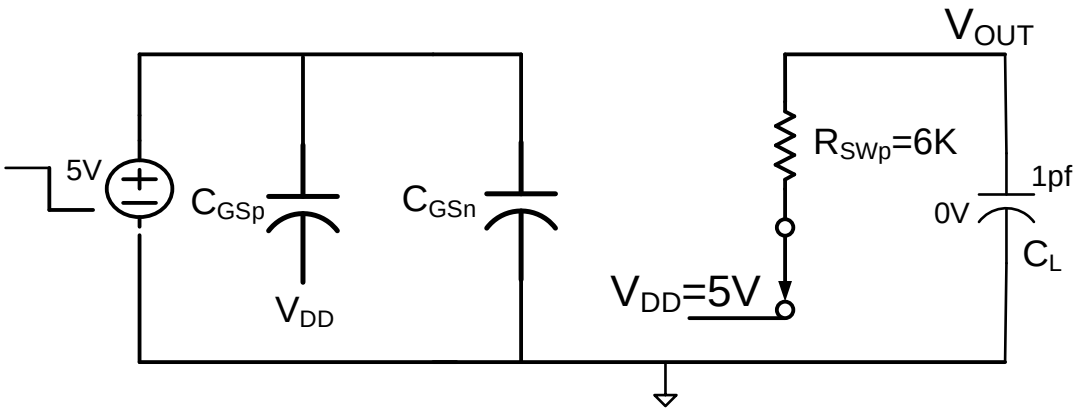


$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

For this circuit, F=5, I=0 and $\tau = R_{SWp}C_L$

Example (cont)

With improved model

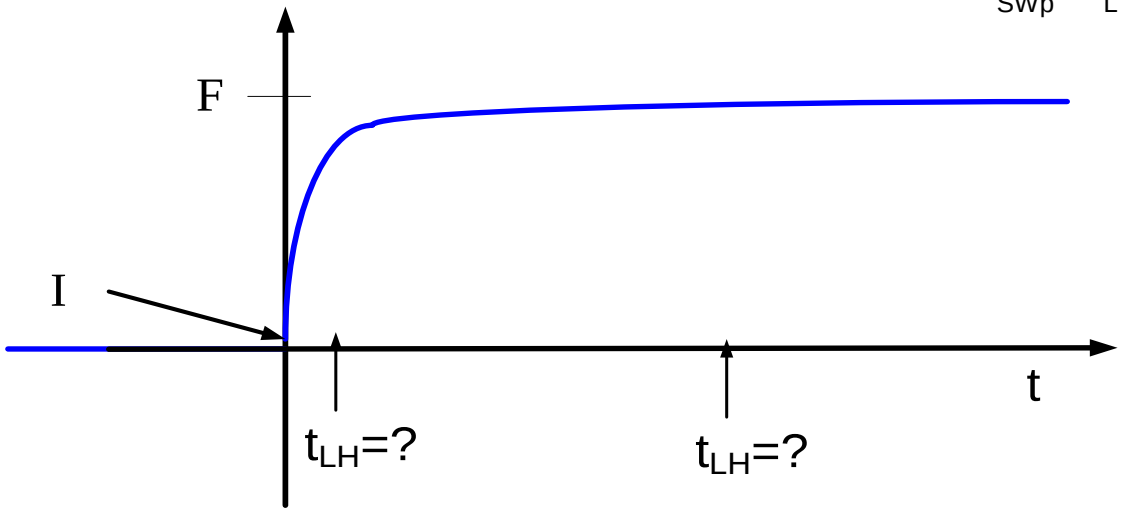


t_{LH}=?

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

$$V_{OUT}(t) = 5\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$\tau = R_{SWp}C_L$$

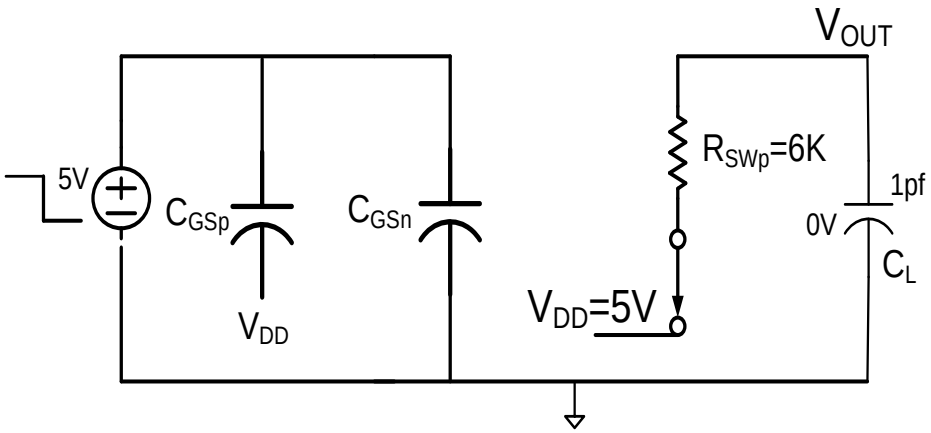


how is t_{LH} defined?

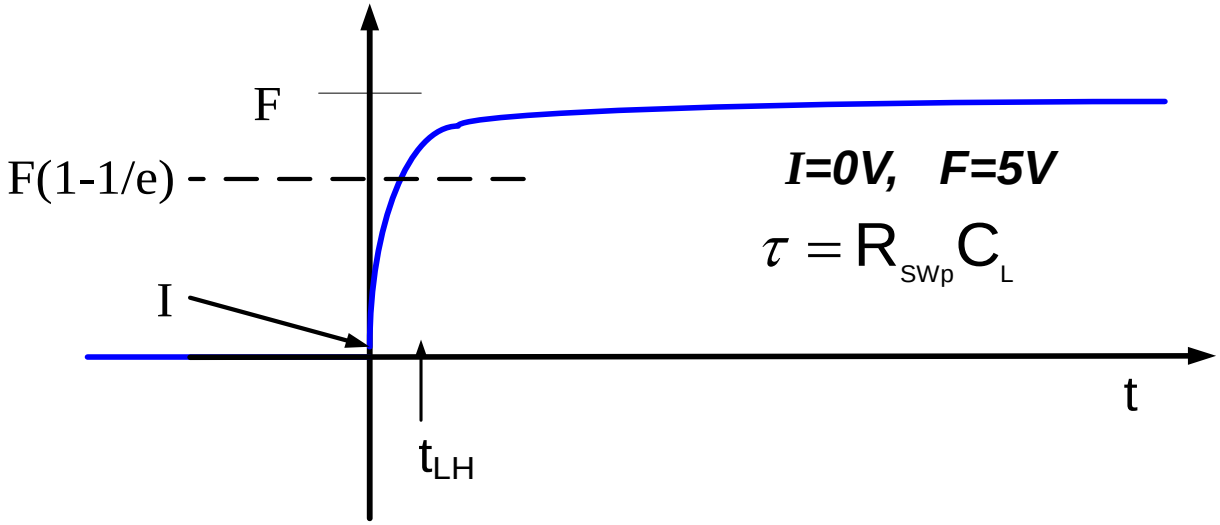
Example (cont)

With improved model

t_{LH}=?



Define t_{LH} as shown on figure



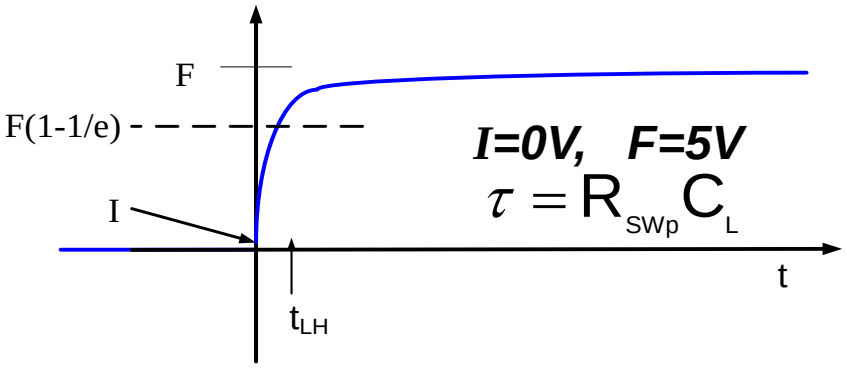
t_{LH} as defined has proven useful for analytically predicting response time of circuits

$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} \quad \Rightarrow \quad F\left(1 - \frac{1}{e}\right) = F + (I - F)e^{-\frac{t_{LH}}{\tau}}$$

Example (cont)

With improved model

t_{LH}=?



$$F\left(1-\frac{1}{e}\right)=F+\left(I-F\right)e^{-\frac{t_{LH}}{\tau}}$$

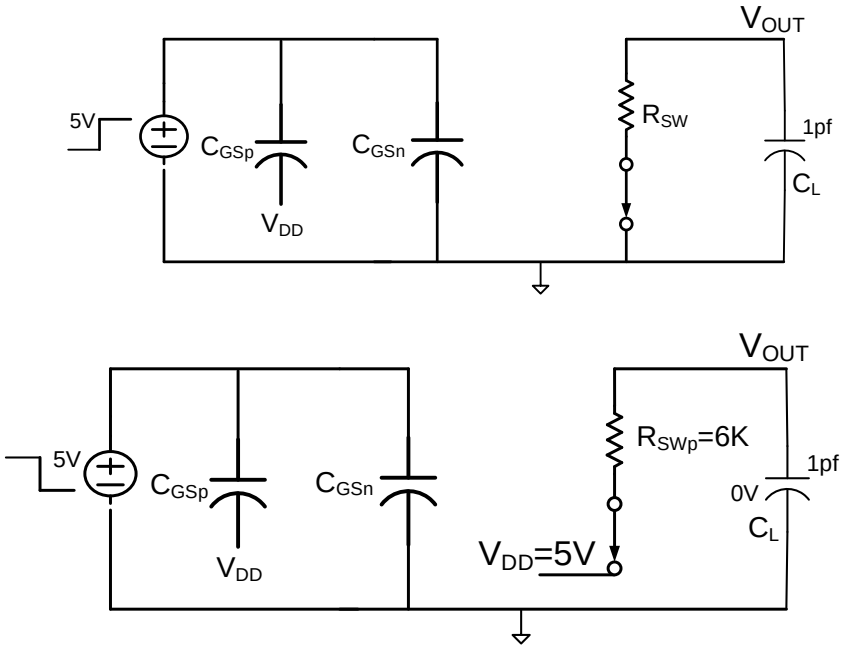
$$F\left(1-\frac{1}{e}\right)=F+\left(F\right)e^{-\frac{t_{LH}}{\tau}}$$

$$1-\frac{1}{e}=1+e^{-\frac{t_{LH}}{\tau}}$$

$$t_{LH}=\tau \quad \Rightarrow \quad t_{LH}=R_{SWp}C_L$$

Example (cont)

With improved model



In the ON 0.5u process

$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 1pF = 2n\,\text{sec}$$

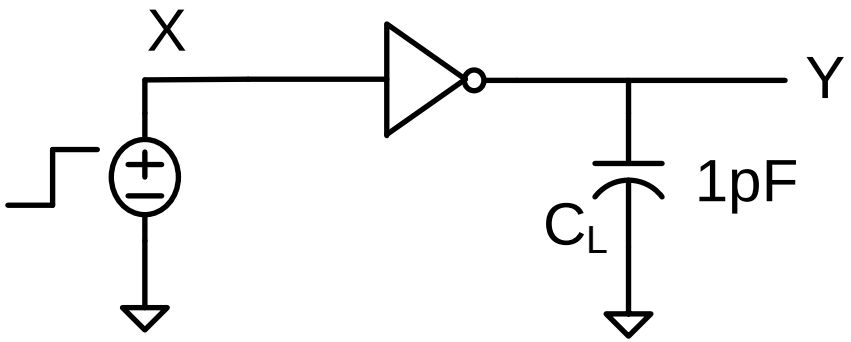
$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 1pF = 6n\,\text{sec}$$

Note this circuit is quite fast !

Note that t_{HL} is much shorter than t_{LH}

Often C_L will be even smaller and the circuit will be much faster !!

Summary: What is the delay of a minimum-sized inverter driving a 1pF load?

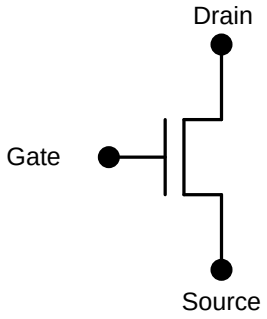


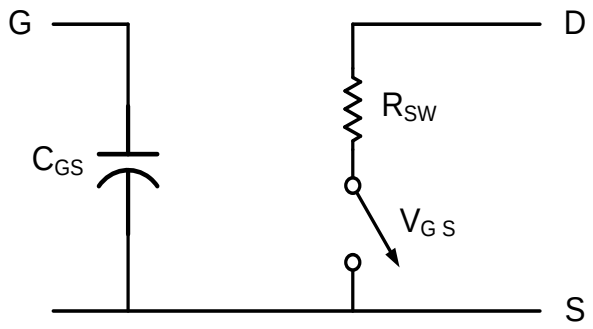
In the ON 0.5µ process

$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 1pF = 2n\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 1pF = 6n\,\text{sec}$$

Improved switch-level model





Switch closed for V_{GS}= large

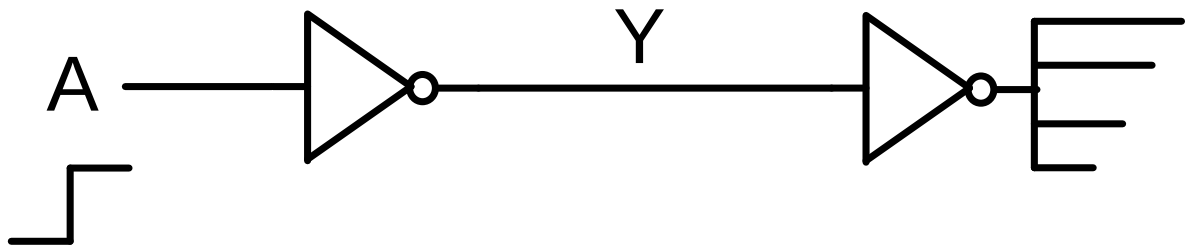
Switch open for V_{GS}= small

- **Previous example showed why R_{SW} in the model was important**
- **But of what use is the C_{GS} which did not enter the previous calculations?**

For minimum-sized devices in a 0.5μ process

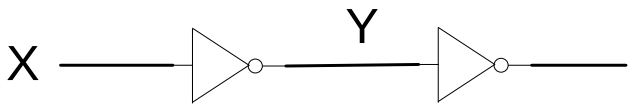
$$C_{GS} \cong 1.5fF \qquad R_{sw} \cong \begin{cases} 2K\Omega \ \ n-channel \\ 6K\Omega \ \ p-channel \end{cases}$$

One gate often drives one or more other gates !



What are t_{HL} and t_{LH}?

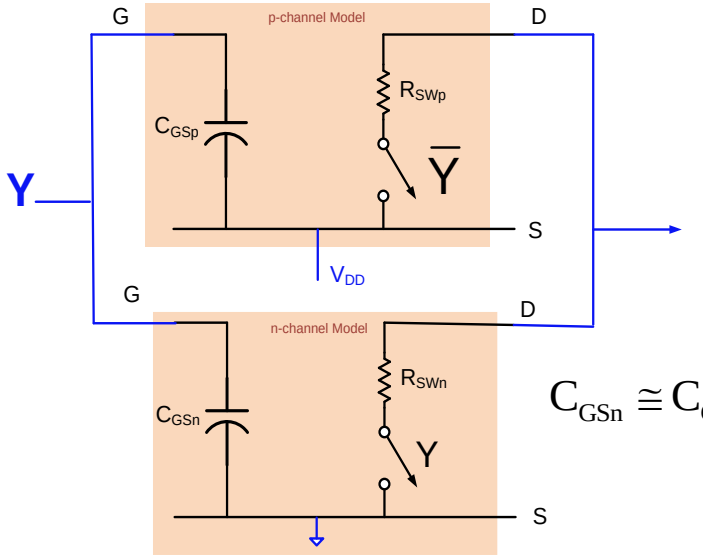
Example: What is the delay of a minimum-sized inverter driving another identical device?



?

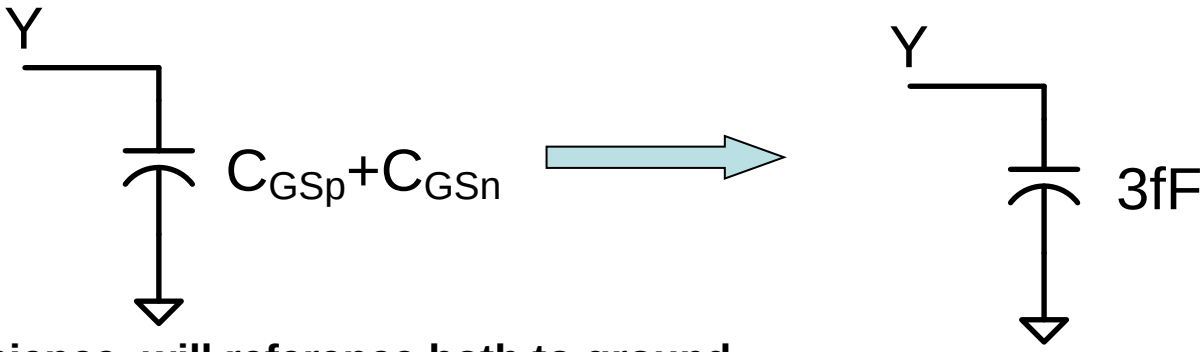
Load on first inverter

C_{GSn} and C_{GSp} both 1.5fF



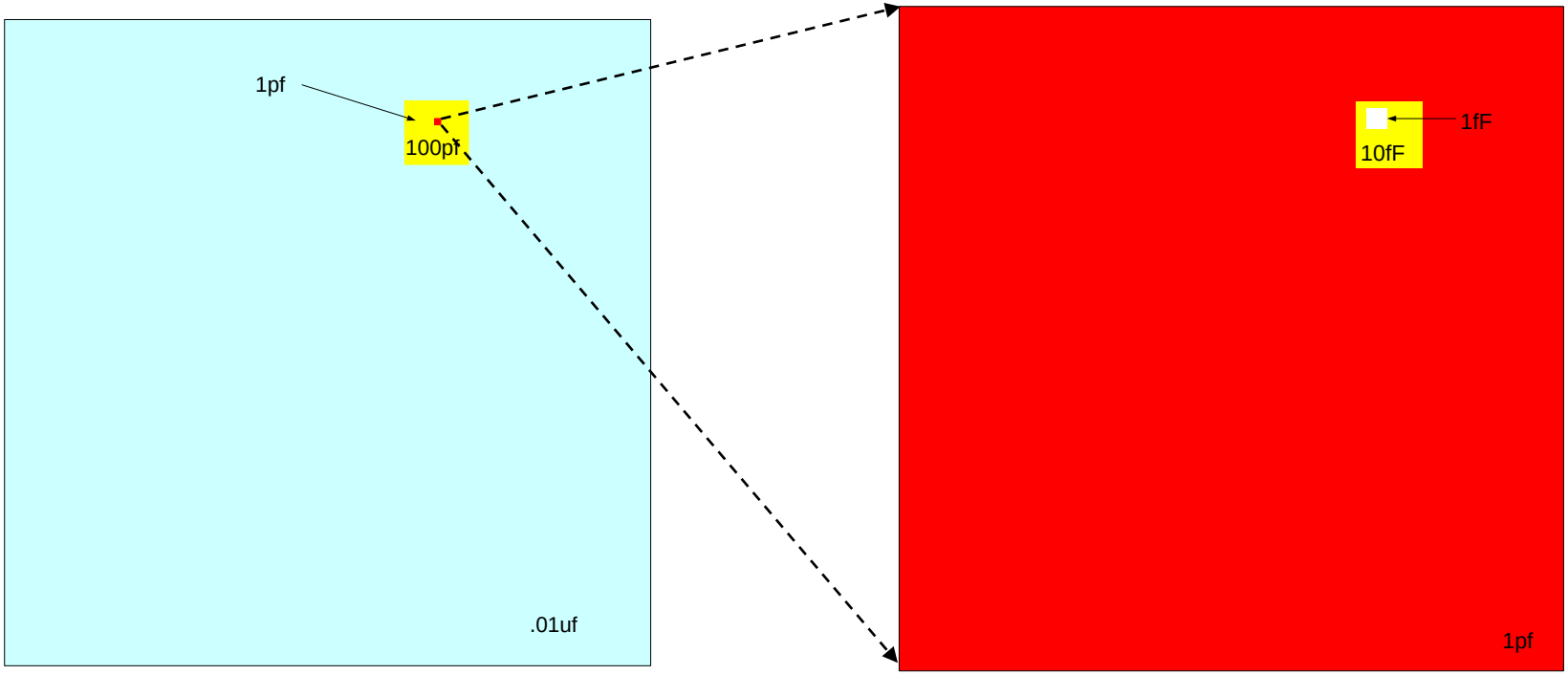
$C_{GSn} \cong C_{GSp} \cong 1.5\text{fF}$

Loading effects same whether C_{GSp} and/or C_{GSn} connected to V_{DD} or GND



For convenience, will reference both to ground

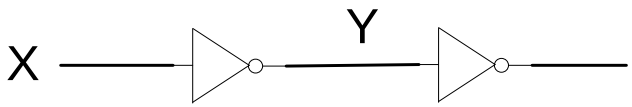
Is a capacitor of 1.5fF small enough to be neglected?

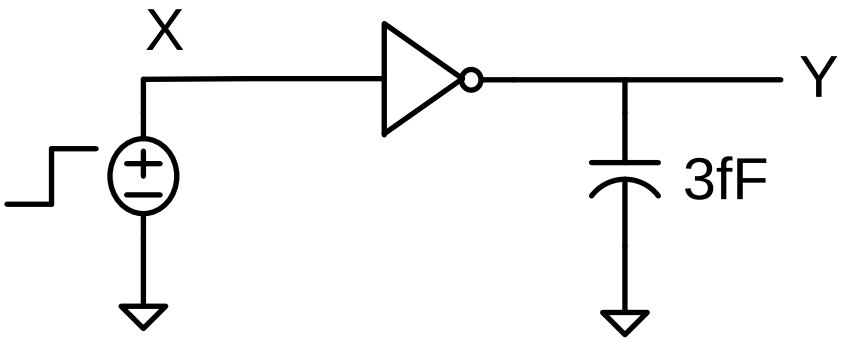


Area allocations shown to relative scale:

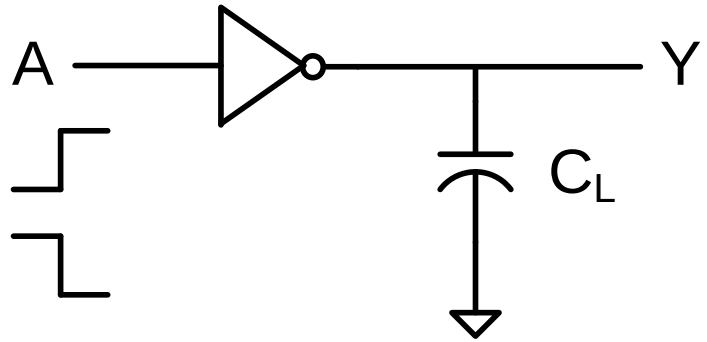
- **This example will provide insight into the answer of the question**

Example: What is the delay of a minimum-sized inverter driving another identical device? Assume V_{DD}=5V





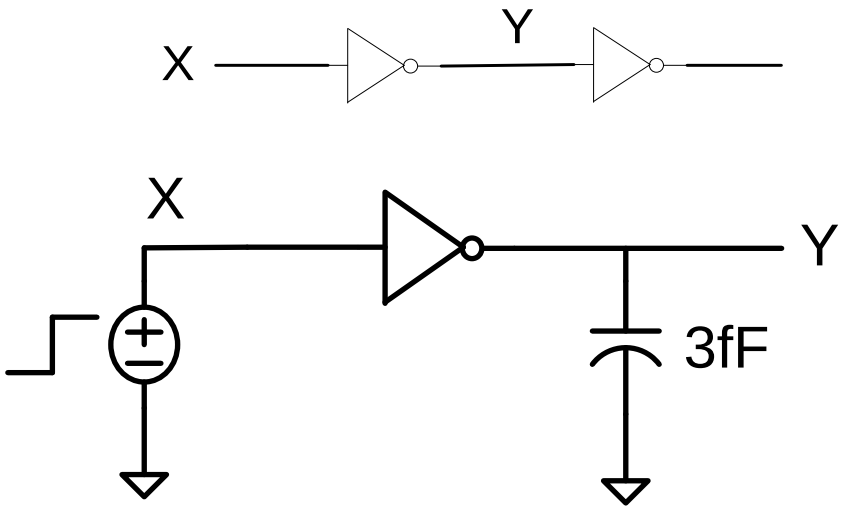
Generalizing the Previous Analysis to Arbitrary Load



$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

Example: What is the delay of a minimum-sized inverter driving another identical device?



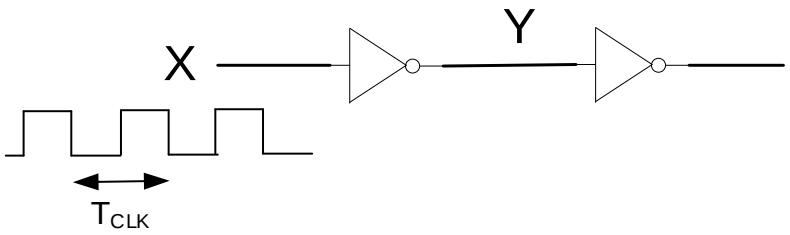
$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 3fF = 6p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 3fF = 18p\,\text{sec}$$

Do gates really operate this fast?

What would be the maximum clock rate for acceptable operation?

Example: What is the delay of a minimum-sized inverter driving another identical device?



$$t_{HL} \cong R_{SWn} C_L = 6p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L = 18p\,\text{sec}$$

What would be the maximum clock rate for acceptable operation?

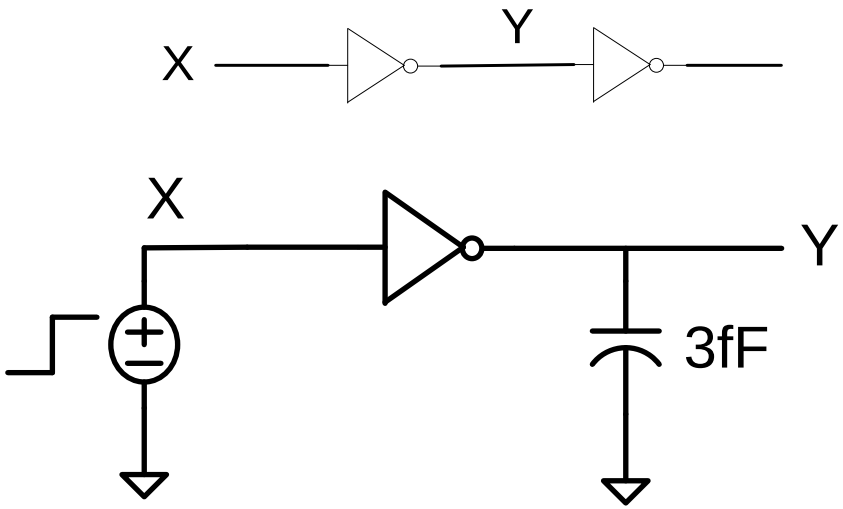
$$T_{CLK\text{-}min} = t_{HL} + t_{LH}$$

$$f_{CLK\text{-}max} = \frac{1}{T_{CLK\text{-}min}} = \frac{1}{24\text{psec}} = 40\text{GHz}$$

And much faster in a finer feature process !! **??????**

What would be the implications of allowing for 10 levels of logic and 10 loads (FanOut=10)?

Example: What is the delay of a minimum-sized inverter driving another identical device? SUMMARY

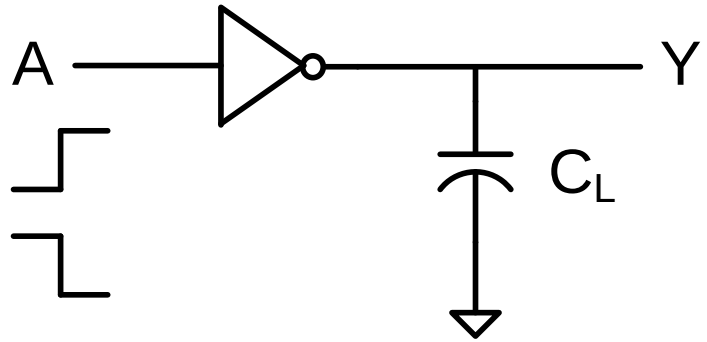


$$t_{HL} \cong R_{SWn} C_L \qquad = 2K \bullet 3\,fF = 6\,p\,\text{sec}$$

$$t_{LH} \cong R_{SWp} C_L \qquad = 6K \bullet 3\,fF = 18\,p\,\text{sec}$$

Note this is very fast but even the small 1.5fF capacitors are not negligable !

Response time of logic gates



$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

- **Logic Circuits can operate very fast**
- **Extremely small parasitic capacitances play key role in speed of a circuit**

Some Observations about Technology and Politics

Technology discussions and laboratory designs in this course will be in an ON 0.5µm process

This technology was State of the Art in about 1995 (25 years ago!)

State of the Art today is about 7nm

Technology Evolution:

1µm, 0.5µm, 0.35, 0.5µm, 0.18 µm , 0.1µm, 90nm, 65nm, 45nm, 28nm, 22nm, 14nm, 10nm, 7nm

11 generations since the 0.5µm process was at the State of the Art

When 0.5µm processes were state of the art, most US researchers and most universities were working with the state of the art processes or maybe one generation behind the state of the art

Some Observations about Technology and Politics

Technology Evolution:

1µm, 0.5µm, 0.35, 0.5µm, 0.18 µm , 0.1µm, 90nm, 65nm, 45nm, 28nm, 22nm, 14nm, 10nm, 7nm

Students at universities in Asia and Europe often have ready access to technologies in the 14nm to 28nm realm

Are we using obsolete technology in US Universities Today?

Why do we not have ready access to "state of the art" technologies in US Universities?

Will students trained with 25 year old technologies be able to work with state of the art technologies?

Are the larger feature size technologies still used by industry today in the US or abroad?

Some Observations about Technology and Politics

US Government has recognized that investment in the semiconductor industry is critical to regain technical dominance in the field

The US is now in a serious catchup position because except for Intel, US technology is now about a decade behind foreign competitors

A recent announcement looks promising for the future !

https://www.washingtonpost.com › 2021/06/14 › global...

Senate approved $52 billion in subsidies for chip manufacturing

Will this investment close the gap that exists today in semiconductor technology or actually reverse the world order in the semiconductor industry?

Some Observations about Technology and Politics

Will this $52 Billion investment by US Government close the gap that exists today in semiconductor technology or actually reverse the world order in the semiconductor industry?

When Pat Gelsinger, the chief executive of U.S. chip giant Intel, visited Europe this spring to scout potential locations for a new factory, officials rolled out the red carpet. European nations are aiming to use part of a 145 billion euro digital fund — about $175 billion — to finance chip investments and double their share of worldwide chip manufacturing by 2030, to 20 percent of the $540 billion global market.

https://www.reuters.com › technology › taiwan-minister-s...

Taiwan's chip industry set for years of growth: minister | Reuters

Apr 23, 2021 — He said between now and 2025, **Taiwan** companies have planned more than T$3 trillion ($107 billion) in **investment** in the **semiconductor** sector, ...

Some Observations about Technology and Politics

Will this $52 Billion investment by US Government close the gap that exists today in semiconductor technology or actually reverse the world order in the semiconductor industry?

https://www.industryweek.com › article › taiwans-tsmc-...

Taiwan's TSMC Plans $100 Billion Investment to Meet Demand

Apr 5, 2021 — **Taiwan Semiconductor** Manufacturing Company said Thursday it was planning to **invest** $100 billion over the next three years to meet soaring ...

South Korea became the latest country to announce a colossal investment in the industry last week. The nation's government said Thursday that **510 trillion South Korean won ($452 billion)** will be invested in chips by 2030, with the bulk of that coming from private companies in the country. May 17, 2021

Samsung Group, South Korea's tech giant, announced on Tuesday that it will invest **$205 billion (240 trillion won)** in their semiconductor, biopharmaceuticals and telecommunications units over the next three years to enhance its global presence and lead in new industries such as next-generation telecommunication and ... Aug 24, 2021

Some Observations about Technology and Politics

Will this $52 Billion investment by US Government close the gap that exists today in semiconductor technology or actually reverse the world order in the semiconductor industry?

https://thediplomat.com › 2020/09 › can-china-become...

Can China Become the World Leader in Semiconductors?

Sep 25, 2020 — **China** appears on track to reach the **investment** level of $150 billion in 2020 without having reached either of its stated long-term goals. And ...

Some Observations about Technology and Politics

Will this $52 Billion investment by US Government close the gap that exists today in semiconductor technology or actually reverse the world order in the semiconductor industry?

Summary of Reported Investments by Some Key Players

Timeframes of investments vary making comparisons sketchy

US Government	$50 Billion
Intel	$100 Billion (over 10 years ?)
European Governments	$175 Billion
Taiwan Government	$107 Billion
TSMC	$100 Billion
Korean Government	$450 Billion
Samsung (included?)	$205 Billion
China	$150 Billion (in 2020 alone)

Some Observations about Technology and Politics

There are serious concerns in the US military that we will not be able to maintain state of the art military systems without domestic state of the art semiconductor technology

The lack of access to state of the art semiconductor technologies in most US universities is primarily driven by the lack of commitment by the US government to support these programs and to support the semiconductor industry to the level of support provided in some other countries

Input on re-establishing priority for governmental support of the US semiconductor industry is critical

Many companies around the world are still using 65nm to 0.5µm technologies for new designs and will for the foreseeable future

Extremely high volume applications of highly complex systems operating at high speeds drive the state of the art technologies

Stay Safe and Stay Healthy !

End of Lecture 7